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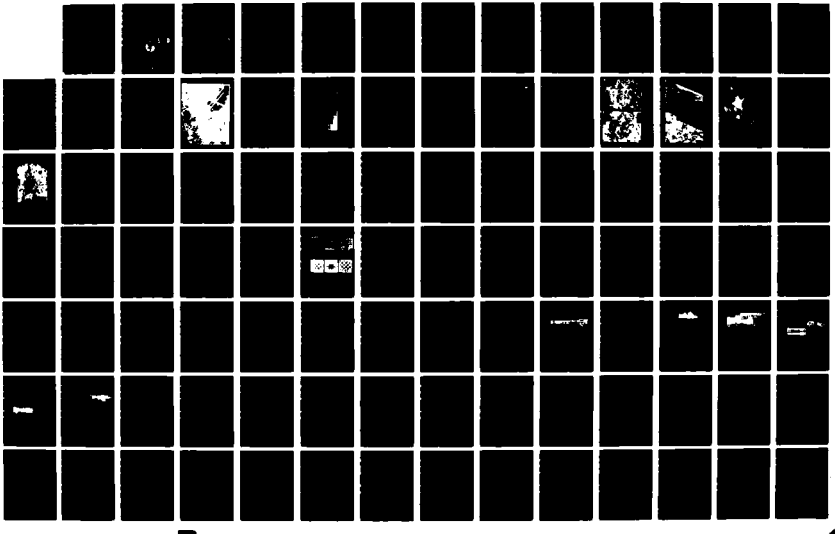

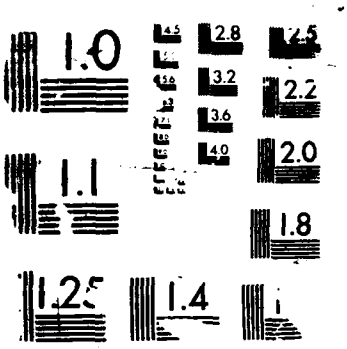

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Semi-Annual Progress Report

on

FUNDAMENTAL STUDIES AND DEVICE DEVELOPMENT IN BETA SILICON CARBIDE

Supported by ONR Under Contract N00014-82-K-0182 P0005

For the Period February 1, 1987 – August 31, 1987

School of Engineering

North Carolina State University

Raleigh, North Carolina

(4)

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The research of this reporting period has involved (1) the CVD of β-SiC on off-axis Si (100), (2) the growth of β- and α-SiC on monocrystalline α-SiC substrates, (3) high temperature ion implantation, and damage production studies, (4) the continued development of contacts for n- and p-type SiC, (5) reactive ion and plasma etching, and (6) the fabrication and evaluation of MESFETs and MOSFETs in β-SiC.

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TABLE OF CONTENTS

I. Introduction

Silicon carbide is the only compound species that exists in the solid state in the Si-C system and can occur in the cubic (C), hexagonal (H) or rhombohedral (R) structures. It is also classified as existing in the beta and alpha modifications. The beta, or cubic, form crystallizes in the zinc blende or sphalerite structure; whereas, a large number (approximately 140) of the alpha occur in the hexagonal or rhombohedral forms known as polytypes.

Because of the emerging need for high temperature, high frequency and high power electronic devices, blue L.E.D.'s, Schottky diodes, U.V. radiation detectors, high temperature photocells and heterojunction devices, silicon carbide is being examined throughout the world for employment as a candidate material in these specialized applications. The electron Hall mobility of high purity undoped β-SiC has been postulated from theoretical calculations to be greater than that of the α-forms over the temperature range of 300–1000K because of the smaller amount of phonon scattering of the cubic material. The energy gap is also less in the β-form (2.3 eV) compared to the α-forms (e.g., 6H = 2.86 eV). Thus, the β-form is now considered more desirable for electronic device applications, and, therefore, improvements in the growth and the characterization of thin films of this material and device development from this material constitute principal and ongoing objectives of this research program.

The research of this reporting period has involved the chemical vapor deposition of β-SiC on off-axis Si (100) and 6H α-SiC and its physical chemical and electrical characterization. We have also grown and characterized 6H α-SiC on off-axis 6H-SiC. Excellent results have been obtained from high temperature ion implantation vis a' vis the reduction in both the damage throughout the profile and the annealing temperature necessary for the maximum possible ionization of the implanted species. Research has also been continued on the development of contacts for both n- and p-type SiC, as well as reactive ion and plasma etching. Finally, extremely encouraging results have been obtained from MESFETs and MOSFETs fabricated in β-SiC films.

The presentation of the information regarding the aforenoted topics will be in the two formats: preprints of papers presented at professional meetings or submitted to refereed journals and additional information in manuscript style which provides linkages between the preprints but which has not yet been submitted for publication. The papers not only summarize the research in 1987 in precise and concise form, but also provide to the reader early access to the forthcoming papers.

II. β-SiC Films on Off-Axis Si (100) Substrate

A. Introduction

Generally, Si (100) is utilized as a substrate for SiC grown by CVD due to its availability and low cost. Unfortunately, β-SiC films grown on Si contain numerous defects, including

antiphase boundaries (APBs). These APBs are generated because a polar compound material, β-SiC is being grown on a non-polar elemental substrate (Si). Due to its non-polar nature, a conventional Si (100) substrate generally contains surface steps of single atomic height. Therefore, when an epitaxial compound semiconductor is grown on such a surface, APBs are created. However, with the proper preparation procedures, the single steps on a conventional non-polar Si (100) surface can be eliminated. This, in turn, eliminates APBs and thereby improves the structural and electrical quality of the β-SiC films as discussed herein.

APBs were observed in CuAu alloys grown on NaCl substrates as early as 1970. They have also been found in various oxide compounds such as BeO and ZnO. However, previous investigations which are most pertinent to the present research involve the growth of polar, compound semiconductors on non-polar substrates. These include GaAs, GaP and β-SiC films on Ge and/or Si substrates. To date the system which has been studied most extensively is GaAs films on Si (100) substrates. The fundamental aspects of APB formation in this system can be directly applied to the β-SiC/Si (100). The structure of Si consists of two interpenetrating Face-Centered Cubic (FCC) sublattices and is generally referred to as a diamond structure. In this structure, the two sublattices are identical except for their spatial locations; one is displaced relative to the other by (1/4 1/4 1/4) of the lattice parameter. On the other hand, GaAs and β-SiC each crystallize in a zinc blende structure which is similar to diamond except that each interpenetrating FCC sublattice is occupied by a different type of atom. For example, in the case of β-SiC, one sublattice contains C atoms and the other Si. When the sublattice atomic occupation is reversed in a crystal with a zinc blende structure, the two dimensional interface which is formed at this reversal is called an antiphase boundary (APB).

Various methods can be used to identify APBs. Relatively simple decoration techniques have been utilized such as etching (both chemical and sputter etching), wet oxidation and Boron decoration. More recently, transmission electron microscopy has been utilized to determine the polarity (i.e., sublattice occupation) of a crystal on either side of an APB. In this case, small deviations from centro-symmetry can clearly and easily be observed by taking advantage of the strong coherent multiple scattering normally present in convergent beam electron diffraction (CBED). For example, the polarity of GaAs has been determined by using the coupling between the weak 200 reflection and two weak odd-index reflections as well as by comparing 200 and $\bar{2}00$ reflections at the zero order Bragg position. CBED has also been used to show the presence of APBs in a β-SiC film on Si.

Several methods of eliminating APBs in thin polar films grown on non-polar substrates have been studied in the literature. Utilizing a non-polar growth orientation such as (211) has been successful in the growth of GaAs films but has caused polycrystallinity in the case of β-SiC films. Careful control of reactant concentrations to enhance exchange reactions during initial stages of nucleation has also been utilized to minimize APBs in gaAs films. Finally, off-axis Si (100) substrate preparation has also been shown to eliminate APBs in both GaAs and SiC films by creating double rather than single surface steps in the Si surface. It is this latter approach which was utilized in the present research to eliminate APBs in SiC and determine the effect of substrate pre-

annealing. Furthermore, the effects of APBs on electrical properties is established and reasons for these effects are postulated based on associated characterization research.

B. Experimental Procedures

Si (100) substrates which were wafered $1^o - 4^o$ off of the [100] direction towards the [011] direction were obtained commercially. These substrates were chemically polished. The substrates were loaded onto the SiC-coated graphite susceptor utilized to hold the samples during chemical vapor deposition. The cold wall vertical, barrel-type rf-heated system described in previous ONR reports, was employed for the deposition. Silane (SiH_4) and ethylene (C_2H_4) were employed as the Si and C sources, respectively, in hydrogen (H_2) carrier gas. Flow rates of the H_2, SiH_4 and C_2H_4 were 3000 sccm, 2.0 sccm and 1.0 sccm, respectively. The growth temperature was approximately 1360°C and the pressure was 1 atm. During certain experiments substrates were pre-annealed at 1030°C for 30 minutes in flowing H_2 (3,000 sccm). This enhanced surface reconstruction, cleaned the surface and relieved residual strains caused by cleaving the wafers to the proper size.

APBs at the surface of the films were easily observed using wet oxidation. Generally, samples were oxidized at 1200°C for 100 minutes at 1 atm in flowing O_2 which was previously bubbled through deionized water. As previous research has shown, APBs are preferentially oxidized *when* H_2O *saturated* O_2 *is utilized.* Therefore, a groove which is easily observed in an optical microscope is created at the APBs. Optical microscopy was also utilized to observe surface morphologies of as grown films utilizing Nomarski phase contrast.

Transmission electron microscopy (TEM) was also utilized to analyze β-SiC films with and without APBs. Plain view TEM samples were prepared by etching away the Si substrate leaving a free standing β-SiC film approximately 10 μm thick. This film was then ion milled from both sides until a small hole appeared. Cross Sectional TEM (XTEM) samples were obtained by sandwiching two samples (including substrates) together with Si supports using epoxy. This sandwich was then mechanically lapped to approximately 2.5 mils and dimpled to ~1 mil using a rotating steel ball coated with diamond paste, perpendicular to the interface. Finally, Ar^+ ion milling was employed until a small hole was observed. An Hitachi H-800 microscope was used for the electron microscopy. Bright field analysis was used largely to observe stacking faults and APBs in the films and dark field analysis was employed to image dislocations within the APBs. Positive identification of the APBs was accomplished with CBED. A 0.1 μm spot size and an accelerating voltage of 75kV were used.

Several electrical measurements were also utilized to characterize the films including Hall effect measurements, differential C-V measurements and Schottky diode evaluation. Prior to these analyses as grown samples were prepared to obtain clean, smooth, reproducible surfaces. First, samples were polished with 0.1 μm diamond paste to reduce surface roughness, followed by a three step cleaning process ((i) Hot H_2SO_4, (ii) Hot 1:1 $NH_4OH + H_2O_2$, (iii) HF) and a deionized

water rinse after each step. Samples were then oxidized in dry, flowing O_2 at 1200°C for 90 minutes to remove polishing damage. Finally, this oxide layer was removed in HF to expose a clean, smooth β-SiC surface.

Hall measurements were conducted using the Van der Pauw method at room temperature. Indium was used for the ohmic contacts to the film. Film thickness was determined by angle lapping the sample and measuring the film in an optical microscope. Carrier concentration vs. depth in the films was determined using a differential C-V method. An LEI Model 2019 Miller Feedback Profiler coupled with a mercury probe station was employed for these measurements. Finally, Schottky diodes were fabricated on the films using 2000Å of thermally evaporated Au. Conventional photolithography employing one dark field mask was utilized to obtain 100 mm diameter dots surrounded by a very large area of Au which served as an ohmic contact. I-V characteristics of the Schottky contacts were measured using an HP 4145A semiconductor parameter analyzer.

C. Results and Discussion

Film surface morphologies were examined by several methods including optical microscopy, profilometry, and Scanning Tunnelling Microscopy (STM). The surfaces of the β-SiC films on the off-axis substrates are smoother than the β-SiC on conventional Si. This is obvious in both the profilometer traces and the optical micrographs. Furthermore, it appears that the film grown on the 4° off-axis substrate and that grown on the 2° off-axis substrate are similar. Scanning Tunnelling Microscope traces from β-SiC films on conventional Si (100) and 4° off-axis Si (100) were also obtained. This data supports the observations from that the films grown on off-Axis Si substrates are smoother than films on conventional Si. Surface smoothness is important in electronic films because rougher surfaces tend to increase leakage current, decrease device transconductance as well as hinder the reproducibility and characterization of electrical contacts. However, even the surfaces of the films grown on 4° off-axis Si (100) were not smooth enough to optimize these properties, thus, all samples were polished prior to electrical measurements as described in the preceeding section. This also allowed for direct comparison of the electrical properties discussed later without any influence of the surface roughness.

Another interesting observation in the optical micrographs was the presence of elongated surface features in the film grown on 4° off-axis Si (100) and perhaps slightly in the film on 2° off-axis Si (100). These elongated features may be due to surface steps (long, parallel features) dominating the surface morphology in the off-axis growth; whereas, stacking faults (small bidirectional features) may dominate the growth on conventional Si. Substrate preannealing has no obvious affect on the as grown surface morphology although as discussed later, it did influence APB formation.

The size and density of the APBs change with the thickness of the SiC films. To determine this, optical micrographs were obtained from samples of different thickness after wet oxidation as described in the preceeding section. The thicker film had a decreased length of APBs at the surface

indicating a decreased area of APBs within the film. The mechanism for this decrease involves the interaction of APBs in the film. When two APBs grow together in the film, they can eliminate each other. In general, the elimination of APBs is energetically favorable since they are defects which have a higher energy than the perfect bulk film. Therefore, if APBs are only generated at the substrate/film interface and not within the film, it is thermodynamically expected that their density would decrease with film growth if an elimination mechanism is present.

As previously mentioned, APBs in β-SiC can be eliminated by growth on Si (100) substrates off-axis towards the [011] direction. This is determined by examining the APB structures in β-SiC films on unannealed Si (100) substrates off-axis by (a) 1°, (b) 2° and (c) 4° towards [011]. For a 1° off-axis substrate, the APB's size and density are reduced but not eliminated whereas for the 4° off-axis substrates they are virtually eliminated. In the case of the 2° substrates, APBs are in general eliminated but still exist at the edges of the film as discussed later. The APBs were eliminated in the films on off-axis substrates due to the formation of double rather than single steps on the substrate surface. These single steps are present due to the non-polar elemental nature of the Si substrate. The APBs form as a result of the polar compound nature of the SiC which is displaced by one atomic distance as it crosses the single step. However, when the Si wafer is prepared off-axis in the [011] direction, double steps are created which do not cause APBs to form. These double steps form because they are thermodynamically favored over single steps as discussed in detail in the literature. In fact, they can be formed even on conventional, on-axis Si (100) surfaces if they are annealed in ultra high vacuum at high temperature for a long time. However, without annealing, the on-axis substrate will not achieve its low energy, equilibrated state and since exact "on-axis" preparation is never truly obtained (i.e., there will always be very slight misorientations), single steps tend to persist.

This can be explained by thermodynamic considerations. Equilibration of the surface and the formation of biatomic steps involves mass transport over the surface with diffusion lengths of the order of $L_d \sim (D_S t)^{1/2}$ where D_S is the diffusion coefficient for surface transport and t is the time. For on-axis substrates, any single steps formed during substrate preparation will be rather spread apart, therefore, long diffusion lengths are required to achieve biatomic step equilibrium conditions. In contrast, 2°–4° off-axis preparation increases the misorientation and thereby decreases the distance between steps. This minimizes the distance over which atoms must diffuse to reach their thermodynamically preferred positions on the biatomic steps. One can imagine that the 1° off-axis substrates are intermediate between the on-axis Si (100) and the 2–4° off-axis substrates. Diffusion lengths are short enough to eliminate some, but not all of the single steps. Therefore, APB size and density is somewhat reduced but not eliminated.

It is worthwhile to mention that the elimination of APBs from films on Si (100) substrates was only accomplished using [011] off-axis directions. When [001] directions were utilized, APBs persisted and films surfaces were quite rough. It should also be noted that large off-axis angles did not yield high quality β-SiC films in this research. Although APBs were eliminated, stacking fault density did not have obvious change.

As previously stated, films grown on 2° off-axis substrates contained APBs near the edges of the sample. These APBs are probably caused by residual strain in the near edge regions of the substrate since cleaving was utilized to achieve the proper substrate dimensions. This residual strain is believed to interfere with the formation of the biatomic steps in this region by balancing the thermodynamic driving force or by persuing single atomic steps which were present. When the substrate was annealed prior to growth to relieve this residual strain, APBs were not observed in the film. Preannealing also helps to clean and reconstruct the surface. However, this is not believed to be the dominant mechanism for the elimination of the APBs in the present case because the APBs were only present close to the cleaved edges of the sample.

Transmission electron microscopy (TEM) was utilized to evaluate the structural quality of the films and examine the APBs. Plan view micrographs were obtained from β-SiC films on Si (100) and 4° off-axis Si (100) substrates. APBs were verified by convergent beam analysis. No APBs were observed in the film grown on 4° off-axis Si (100) although stacking fault density did not seem to be affected by growth on off-axis substrates. However, it is interesting to note that some stacking faults are slightly misoriented from their expected directions. This is not simply due to sample bending because in certain cases this misorientation is observed between overlapping faults. The cause of this phenomenon is currently under investigation.

If the APBs in a β-SiC film on on-axis Si (100) are examined more closely it is found that they contain a very high density of dislocations. The dislocation density in these APBs is approximately 2 x 10^5/cm which corresponds to an average of one dislocation every 500Å. As was obvious from the microscopy, the density in the APBs is much higher than the density in the rest of the film. This increased density is believed to be caused by the misfit created at the APBs similar to well known misfit dislocations at substrate-film interfaces. In the case of APBs, the misfit is caused by the relative differences in bond lengths between Si-Si and Si-C, C-C and Si-C, and Si-Si and C-C which are 24.3%, 18.5% and 34.5%, respectively. That is, at an APB there will be Si-Si and/or C-C bonds present which give rise to tensile and compressive stresses in the film, respectively, since the bulk of the structure consists of only Si-C bonds. Therefore dislocations are created to relieve some of this stress. The situation is complicated by the fact that different bond types will be present in the APBs depending on the plane in which an APB lies. For instance, in a {110} APB, equal numbers of Si-Si and C-C bonds will be present whereas in a {100} APB, either Si-Si or C-C bonds will dominate. In fact, it is quite probable that the APBs consist of steps which mix the Si-Si and C-C bonds – and therefore the tensile and compressive stresses – in order to lower the energy of the APB. The misfit dislocations then lower the energy further.

The primary application for these films is for electronic devices, therefore, it is of interest to determine the effect of the elimination of the APBs on various electrical properties. Hall measurements indicated that the samples on 4° off-axis substrates were n-type with similar resistivities (0.10 – 0.6 Ω-cm) as those on exact Si (100) substrates. Furthermore, Hall electron mobilities ranged from 200 to 400 cm^2/V-s also similar to films on exact Si (100), although significant scatter in mobility data makes this comparison somewhat tentative. However, utilizing differential C-V measurements several differences were observed. The carrier concentrations in the β-SiC on 4°

off-axis Si were one and one half to three times lower than films on exact Si (100). Although significant variations in carrier concentration can occur from one growth run to another, this is believed to be a real affect because within a single run, average carrier concentrations always indicated the same result. Measured values for the films on 2°–4° off-axis substrates were in the range of 1–10 x $10^{16}/cm^3$. It was also found that the allowable applied voltage for accurate C-V measurements was greater for the films on off-axis substrates. This indicates lower leakage currents for these samples and allows the carrier concentration to be measured to greater depths in the sample. Generally, 3–5 volts could be applied to a film on exact Si (100) whereas more than 10 volts could be applied to the films on off-axis Si.

Au-β-SiC Schottky barrier diodes were fabricated on the β-SiC films to further evaluate their electrical properties. As with the C-V examination, this data indicates that eliminating APBs significantly reduces the leakage current in the film. Leakage currents as low as 2.55 x 10^{-2} A/cm^2 at a reverse bias of 18 V have been achieved for diodes in films on off-axis Si. This decrease in leakage current when APBs are eliminated is attributed to the secondary defects associated with the APBs. As previously shown, APBs contain numerous dislocations which may act as a leakage channel during electrical measurements. Furthermore, many stacking faults intersect the APBs at various points, therefore, the APBs act as a connecting channel for these faults. Finally, local changes in electronic structure at the APBs causing resistivity and/or carrier concentration changes are also possible. Regardless of the mechanism of this leakage current decrease, it indicates that devices fabricated in a film on off-axis Si (100) substrates will be of higher quality than those fabricated on exact Si (100). Such devices are currently under investigation and will be compared with previous device results from films on exact Si (100) from the authors' laboratory.

The I-V data of an Au-β-SiC Schottky diode fabricated on a film grown on a 4° off-axis substrate was plotted in a semi-logarithmic manner. From the slope of the linear portion of the plot, the ideality factor, n, was found to be approximately 1.4. The saturation current, I_s, determined from the extrapolated intersection of this plot with the current axis is 1.53 x $10^{-8}A/cm^2$.

D. Summary of Section II

Beta-SiC films have been grown on Si (100) substrates off-axis towards the [011] direction. Various characterizations were also accomplished and compared with films grown on "on-axis" or "exact" Si (100) substrates. It was found that APBs were essentially eliminated from films grown on 4° off-axis substrates, whereas, they persisted in films on 1° off-axis substrates. When 2° off-axis substrates were utilized, APBs were present in the near edge regions of the sample but these were eliminated by substrate preannealing. This is believed to be related to strain induced during cleaving of the substrates which was relieved during preannealing. It was also found that films were significantly smoother than those grown on exact Si (100) substrates. Stacking fault density appeared to be unaffected by the use of off-axis substrates. Electrical measurements indicated that undoped films on off-axis substrates were n-type with carrier concentrations in the range of 1–10 x $10^{16}/cm^3$, usually one to three times lower than similar films on exact Si (100) substrates. Hall mobility of the films were in the same range, regardless of substrate orientation, although signifi-

cant scatter in this data made comparisons difficult. Au Schottky diodes fabricated in these films on 4° off-axis substrates yielded an ideality factor of 1.4 and a saturation current of $1.53 \times 10^{-8} A/cm^2$. Leakage current was found to be significantly reduced in the films on 4° off-axis substrates indicating better device quality should be achievable. An investigation of devices in these films is currently ongoing.

III. Beta-SiC Films on Alpha-SiC Substrates

A. Introduction

A continuing problem with the CVD growth of β-SiC is the use of a suitable substrate. Silicon (100) is the most widely utilized substrate material, but its lattice parameter mismatch with β-SiC (~20%) and differences in thermal coefficients of expansion (~8% at 473 K) cause β-SiC films grown on Si to contain numerous defects.[1] Titanium Carbide (TiC) has also been employed as a substrate material for β-SiC due to much better lattice matching. Unfortunately, high quality single crystals of TiC are virtually non-existent although research at Hughes Research Laboratories may soon rectify this problem[2]. Another choice of substrate has recently been off-axis Si (100) towards [011] which has been shown to be very effective in GaAs CVD and was discussed earlier in this report. However, when utilized for the growth of β-SiC, only the antiphase domains are eliminated, whereas stacking faults, dislocations and elastic strain still persist in the film regardless of the degree of misorientation of the substrate.

Obviously, the best substrate/film matching would be obtained by utilizing SiC substrates. Unfortunately, high purity, defect free bulk SiC has not been available on a regular basis. The primary source for these crystals at present is the random growth of alpha-SiC in commercial Acheson furnaces used to make SiC grit for abrasive applications. However, recent research into the growth of high purity, bulk alpha-SiC crystals via modified Lely method appears promising.[3,4] Therefore, the feasibility of using SiC as a substrate for the CVD of β-SiC thin films is currently under investigation and is the impetus for the research presented in this section.

For the present study, β-SiC films were grown on α-SiC crystals obtained from an Acheson furnace and were characterized using X-ray topography as well as X-ray rocking curve analysis and transmission electron microscopy (TEM). The major advantage of the X-ray techniques is their large area/volume nature as compared to the small area/volume nature of TEM. The X-ray analyses have allowed the observation and identification of defects not observed during cross sectional TEM (XTEM) research. It should be stressed that the X-ray techniques, which are large volume, low resolution techniques, compliment the high resolution, small volume nature of the transmission electron microscopy.

B. Experimental Procedures

Beta-SiC thin films were epitaxially grown on (0001) alpha-SiC substrates via CVD. Substrates were obtained from an Acheson furnace and had natural {0001} type as grown surfaces. Since SiC is a polar material, these natural surfaces can terminate in either a Si layer (0001) or C layer (000$\bar{1}$) and a thin crystal with two parallel, smooth surfaces will contain one Si face and one C face opposite to each other. However, the Acheson derived crystals generally contain only one flat surface which is usually Si. To prepare a clean surface, substrates were preoxidized at 1473K in a flowing dry oxygen atmosphere for 90 minutes which removed approximately 50 nm of the as grown surfaces. Furthermore, by estimating oxide thickness on both {0001} type faces, the polarity of the natural surface was determined since the oxidation rate of the C face is quicker than that of the Si face. The resulting oxide layer was removed using 49% hydrofloric acid immediately prior to loading the sample onto the SiC-coated graphite susceptor utilized to hold the samples during CVD growth. The cold wall, vertical barrel-type, rf-heated system, described in numerous previous reports to ONR, was employed for the deposition.

The substrates were initially heated at the growth temperature, which varied between 1683–1823 K, for 10 minutes in 1 atm of flowing H_2 (3000 sccm) to perform high temperature cleaning and to etch the native oxide on the SiC surface. The reactive gases of SiH_4 and C_2H_4 were subsequently introduced into the H_2 stream to start SiC deposition under the same temperature and total pressure. The SiH_4/C_2H_4 flow rate ratio was 2. The ratio of the sum of the flow rates (sccm) of SiH_4 and C_2H_4 to the flow rate (sccm) of H_2 was 1:3000. The particular sample examined in this research was grown at 1773 K for 3 hours on the Si face of the α-SiC substrate. The as grown surface of β-SiC grown on the C face is much rougher under the same growth conditions, however, both as-grown surfaces contain the mosaic structure described later.

A Rigaku rotating anode X-ray unit and CuK_α radiation were used in this study. The X-ray tube was operated at 35 KV and 20 mA. A Lang camera capable of scanning the crystal and a photographic plate past a tall narrow beam of X-rays allowed large areas of the crystal to be examined. The horizontal divergence of the incident CuK_α beam was limited by a slit at the end of a collimating tube and was less than one minute of arc for this research. This divergence resulted in the Full Width at Half Maximum (FWHM) of a (220) rocking curve for a near perfect Si crystal to be approximately 1.5 minutes of arc.

Scanning reflection X-Ray Topography (XRT) was used to examine the β-SiC thin film and 6H SiC substrate structural quality over the entire area of the sample. Although the lattice mismatch at the β-SiC/α-SiC interface is very small, the crystal perfection of the substrate and the β-SiC epilayer can be studied independently with this XRT system. Furthermore, rocking curve analysis was used to calculate the lattice mismatch between the substrate and the epilayer. The experimental arrangement of the XRT system is depicted in Figure 1. The reflected beam is perpendicular to the photographic plate or Geiger tube detector used for rocking curve scans. Ilford nuclear plates, type L4, with emulsion 24 μm thick were used to record the scanning XRT images. The (222) and (331) planes of β-SiC were chosen as reflection planes, since they have relatively

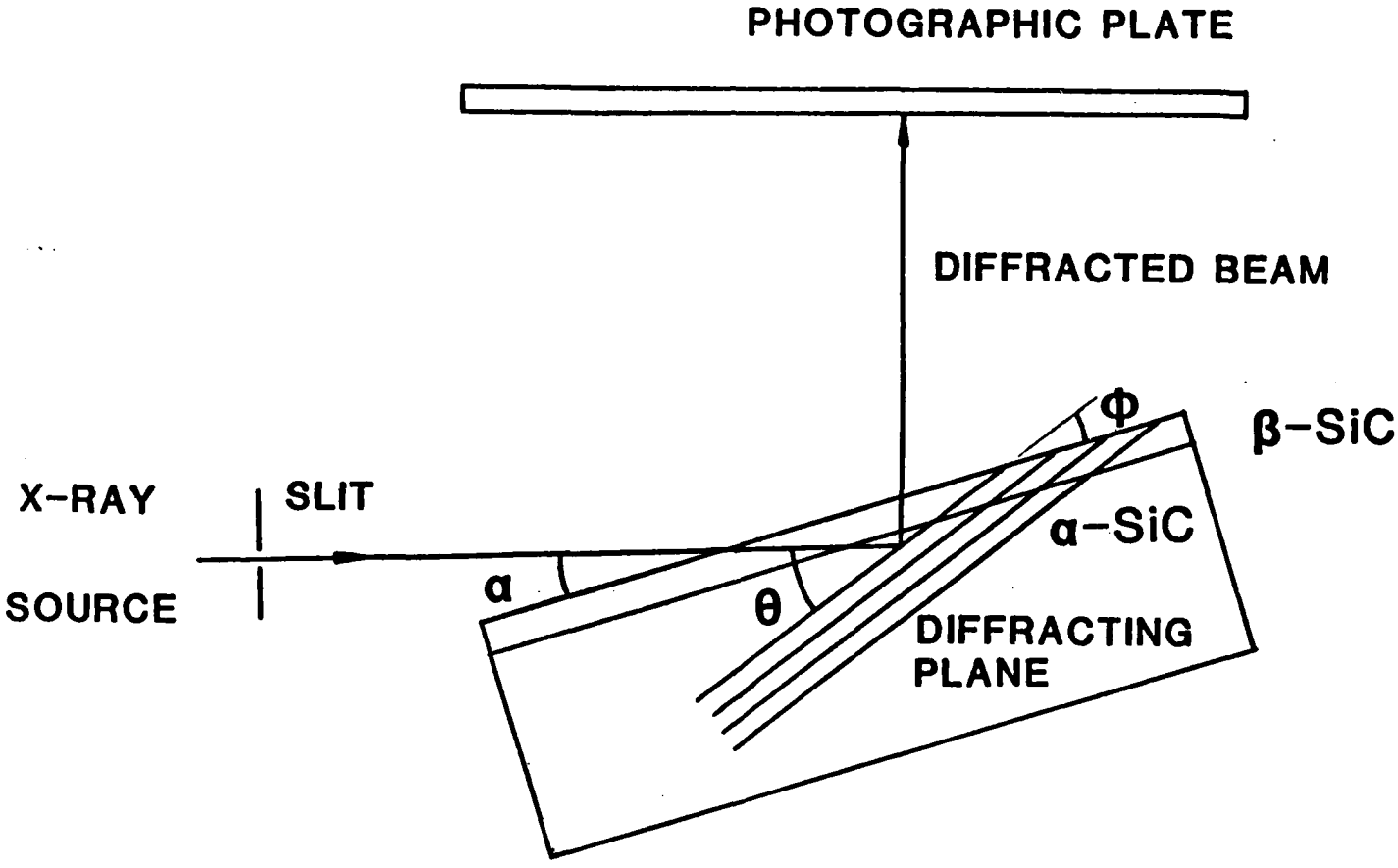


Figure 1. Schematic of X-ray topography configuration.

large Bragg angles and strong diffraction which allow the separation of the diffracted beams from the epilayer and the substrate.

As a complimentary method to XRT, Transmission Electron Microscopy (TEM) was used to observe the defects in the β-SiC thin films. For plan view examination, samples were mechanically lapped from the back side (substrate side) with diamond paste to about 2.5 mils. They were then dimpled to approximately 1 mil in the center. Finally, Ar^+ ion milling was employed to thin the sample from the back side until a small hole was observed. An Hitachi H-800 TEM was then utilized for the microscopic examination. For cross-sectional TEM (XTEM) samples, similar preparation methods were employed perpendicular to the plane of the film after "sandwiching" two samples together with Si supports using epoxy.

C. Results

(1) β-SiC Films on α-SiC Substrates vs. Si Substrates

As mentioned previously, the most widely utilized substrate material for the CVD growth of β-SiC is currently Si (100). However, its lattice parameter mismatch with β-SiC and differences in thermal coefficients of expansion cause β-SiC films on Si to contain numerous defects. This is illustrated in Figure 2 which is a cross-sectional transmission electron micrograph of the β-SiC/Si interface. The extremely high defect density at the interface extends ~3 μm into the film, however, many defects propagate all the way to the as grown surface. Stacking faults, dislocations and antiphase domains (marked with arrows) can be seen in this figure. Furthermore, contours indicating the presence of elastic strain are visible near the interface. X-ray rocking curve analysis can also be used to evaluate the elastically strained nature of β-SiC grown on Si (100). This was accomplished by examining the β-SiC film before and after removing its Si substrate. This is shown in Figure 3 for a 14 μm thick film. The removal of the Si substrate (via etching in an $HF:HNO_3$ – 1:1 solution) caused the FWHM to decrease from 15 minutes to 8.6 minutes. This is due entirely to the relief of elastic strain in the sample since other defects will not be affected by simply removing the Si substrate.

In contrast, β-SiC films grown on α-SiC (0001) contain a much lower defect density. In fact, during XTEM evaluation it was generally found that few interface defects could be located and only several defects in the bulk of the film were observed in a particular sample. An XTEM micrograph from such a sample is shown in Figure 4, which when compared to Figure 1, illustrates the drastic difference between films grown on α-SiC (0001) vs. Si (100). However, it should be realized that the small sampling volume of TEM analyses coupled with the fact that XTEM examines only the cross-sectional nature of the film, can lead to erroneous conclusions about defect structures in the film. Therefore, X-ray rocking curve analysis and topography were utilized as discussed below, to provide a more complete understanding of β-SiC films on α-SiC substrates.

Figure 2. XTEM micrograph of single crystal, undoped CVD β-SiC deposited on Si(100) substrate. g = [022].

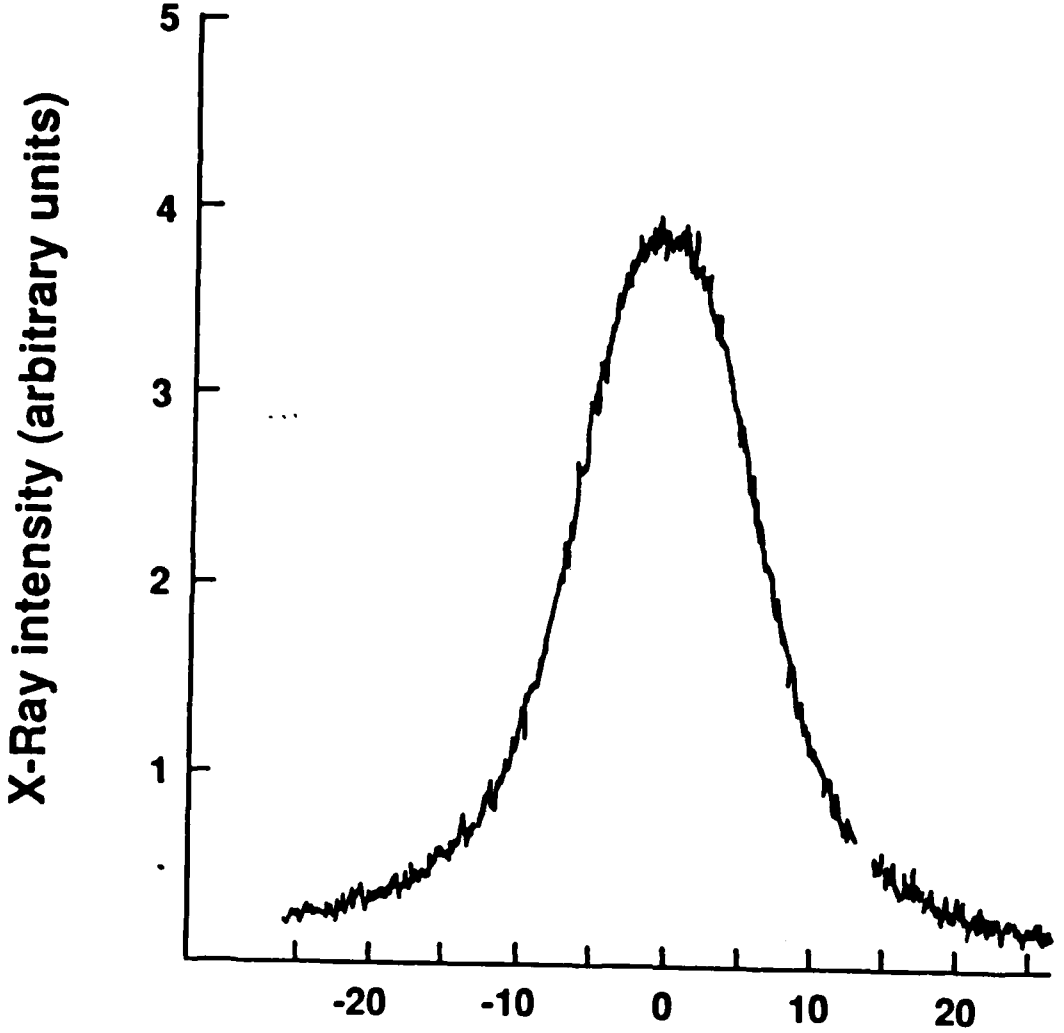
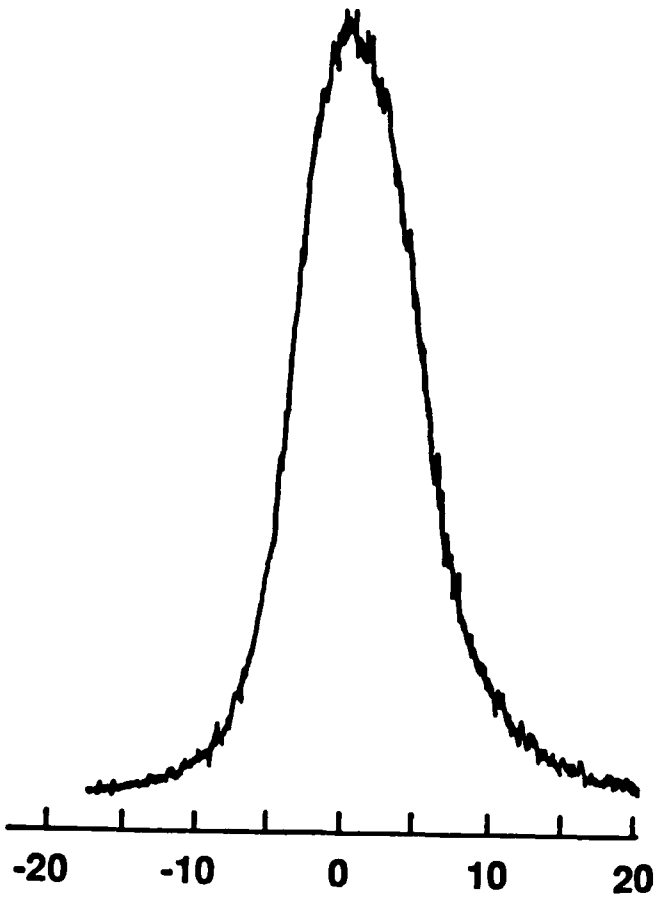


Figure 3a. Rocking curves obtained from β-SiC grown on Si(100) substrate g-[200] before etching Si substrate.



θ (arc minutes)

Figure 3b. Rocking curves obtained from β-SiC grown on Si(100) substrate g - [200] after etching away Si substrate.

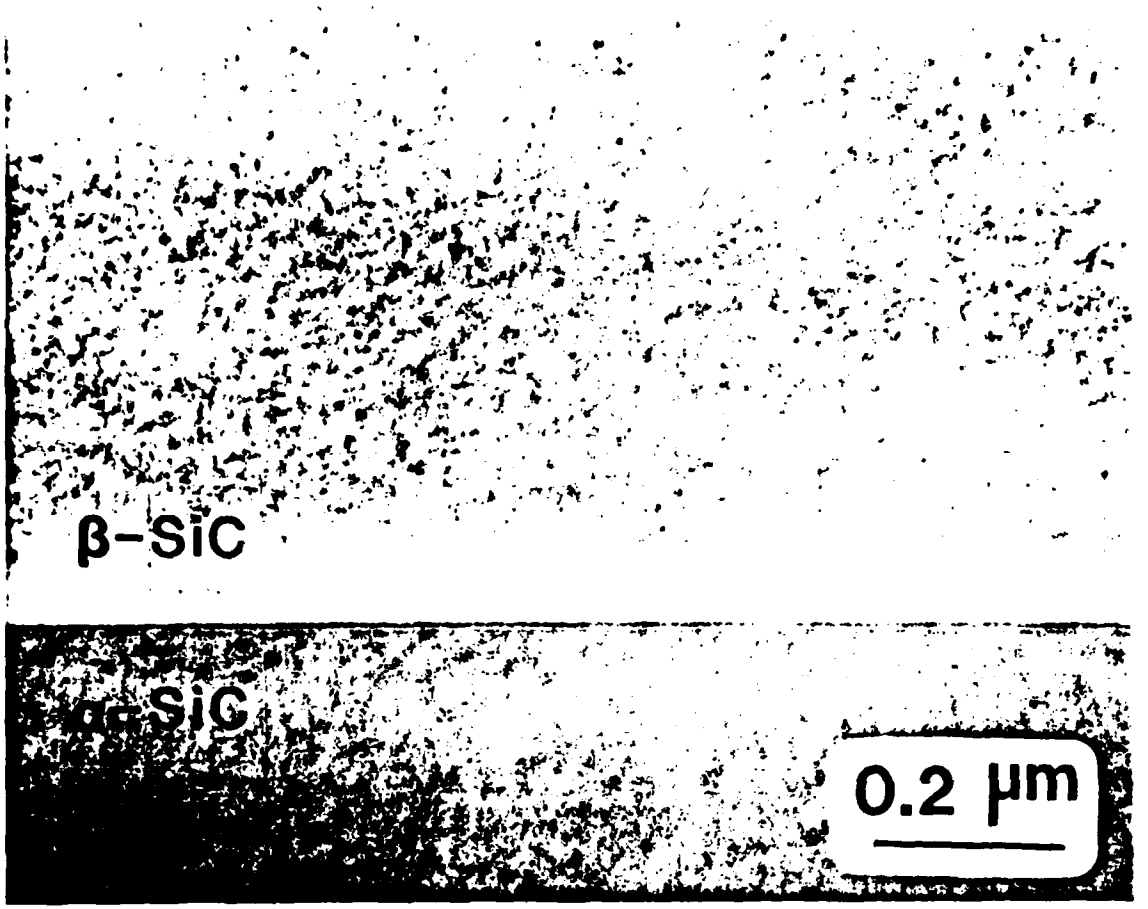


Figure 4. XTEM micrograph of the β-SiC deposited on 6H SiC. Electron beam is parallel to [101] direction of β-SiC.

(2) α-SiC Substrate/β-SiC Film Misfit

Although XTEM indicates a coherent, nearly perfect interface, it is none the less expected that a finite misfit exists between the substrate and the film since they are different crystal structures (hexagonal (6H) vs. cubic (zincblende), respectively) and because they contain different impurity concentrations (the Acheson derived substrates generally contain nitrogen and aluminum impurities). Therefore, X-ray rocking curve analysis (Figure 5) was used to quantatively assess this misfit. Two pairs of diffraction peaks appear in this figure due to the $CuK_{\alpha 1}$ and $CuK_{\alpha 2}$ characteristic lines. In each pair, one peak is from the epilayer, while the other is from the substrate. In this experiment, the (222) reflection from the β-SiC film and the (00012) reflection from the 6H SiC substrate are in the Bragg diffraction condition.

The lattice misfit between the two planes of the two materials can be readily calculated from this curve by a simple manipulation of Bragg's law,

$$|f| = |(d_\beta - d_\alpha)/d_\alpha| = \cot \Theta \cdot \Delta\Theta$$

where f is the misfit, d_β and d_α are the lattice interplanar spacings for β-SiC and 6H SiC, respectively; Θ is the Bragg angle of the (222) reflection of the epilayer; $\Delta\Theta$ is the angular spacing between the peak of the substrate and that of the epilayer in the rocking curve. In this case, considering $CuK_{\alpha 1}$ radiation, $\Theta = 37.58°$ and $\Delta\Theta = 2'$, which yields a lattice misfit of 7.6×10^{-4} or 0.076%. Therefore, despite the impurities in the substrate, especially aluminum ($1–10 \times 10^{19}/cm^3$) and nitrogen ($1–10 \times 10^{18}/cm^3$) and the different crystal structures of the film and substrate, the overall misfit is quite small, thus yielding the coherent interface already discussed in relation to Figure 4.

(3) Domains and Boundaries in a β-SiC Film on an α-SiC Substrate

An optical micrograph of the typical surface morphology of a β-SiC thin film grown on the natural Si surface of a 6H SiC substrate is shown in Figure 6. This type of surface morphology has also been reported by other researchers[5,6] and has been referred to as a mosaic structure. However, the nature of this pattern and its origin were unknown. In the present research, XRT and plan view TEM were employed to study the exact nature and cause of this mosaic pattern, as well as identify other defect structures in the film as discussed below.

Although the mosaic morphology may easily be misinterpreted as simple growth steps or ledges, initial plan view TEM results indicated that boundaries existed in the film across which different and distinct orientations were observed. Therefore, it was naturally suspected that these boundaries caused this mosaic pattern. Consequently, an XRT examination of the film was conducted to unambiguously evaluate this orientational relationship over large areas of the film and directly compare this to the optical observation of the mosaic structure.

The sample utilized for the surface morphology study in Figure 6 was mounted on the XRT stage with tape, and was adjusted such that the (331) plane of the β-SiC film was in the Bragg

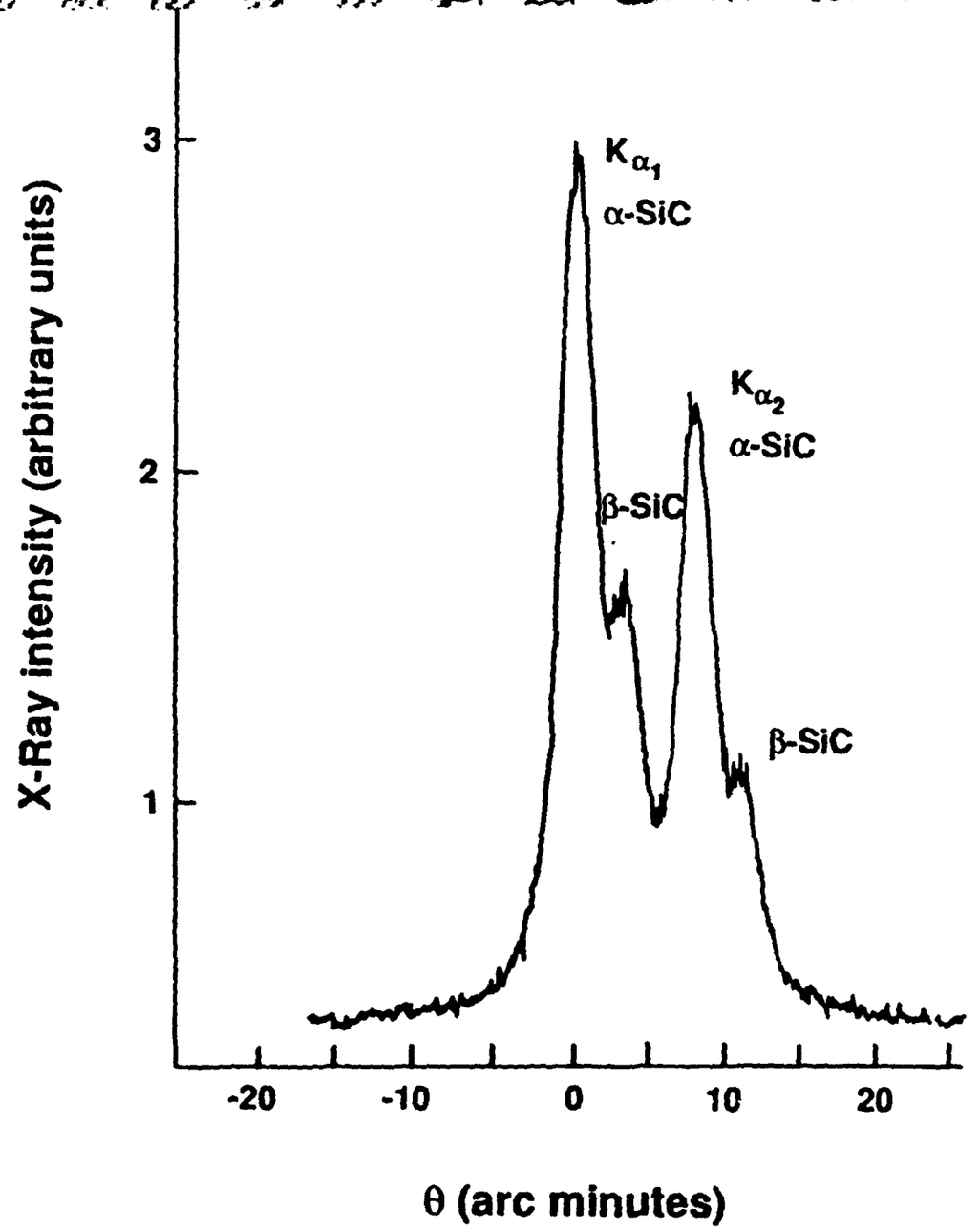


Figure 5. Rocking curve of β-SiC on 6H SiC.

Figure 6. Nomarsky micrograph of surface morphology of a as grown β-SiC thin film on 6H SiC.

diffraction condition. A topograph (Figure 7(a)) was then taken for 2 hours. It was found that some areas of the β-SiC film were in a diffracting condition (dark areas) and that the other areas were not (bright areas). The sample, was then rotated 60° around its [111] axis, while all other conditions remained constant. Another topograph was then taken as shown in Figure 7(b). It can be seen by comparing Figures 7(a) and 7(b) that the diffracting and non-diffracting areas were exactly reversed by this manipulation. This indicates that regions in the β-SiC film corresponding to the dark areas in the topograph are rotated 60° around the [111] axis relative to the regions in the β-SiC film corresponding to light areas in the topograph. Thus, these regions or "domains" are, in fact, twins and the boundaries between them are a special type of incoherent twin boundary. The twin axis is the [111] direction, however, contrary to conventional twinning, there is no mirror plane associated with these structures. The twin axis has two-fold rotational symmetry, but it coincides the [111] axis which has three-fold rotational symmetry, which creates the 60° relative rotation between the domains.

All of the twin boundaries form closed domains although some contain islands of material rotated 60° within them as seen in Figure 7. The sizes of the twins range from one tenth of a micron to hundreds of microns. They also exist in a variety of irregular shapes as well as in fairly regular triangles. Generally, traces of the boundaries are aligned along ⟨110⟩ directions.

If the optical micrograph in Figure 6 is now compared to the X-ray topograph in Figure 7, a direct mirror image is observed. Thus, the morphological features observed optically are caused by the twin boundaries discussed above. It should be noted that the boundaries themselves are observed rather than the actual twins. This is unlike the case of conventional twins which are observed using optical contrast caused by their different orientations and consequently different reflection characteristics. Furthermore, in the special twins discussed here, the boundaries are not the low energy, coherent boundaries associated with conventional twins. In many cases, V-shaped grooves, microcracks and/or steps are associated with these boundaries at the film surface, thus causing sufficient optical contrast with the surrounding smooth, flat surface to be observed in a low magnification optical micrograph. These features indicate the rather high energy nature of these boundaries as further evidenced by features observed in the plan view TEM samples discussed later. It should be noted that the mirror relationship between the optical micrograph and the XRT is caused simply by the reflection type of X-ray topography method used in this research which gives a mirror image of the real features.

In order to determine if the twins were an extension of similar structures in the substrate, a topograph of the (2$\bar{1}$$\bar{3}$2) diffraction plane of the 6H SiC substrate was taken (Figure 8(a)). This diffraction condition, which minimizes the influence of the β-SiC film on the topograph, indicates that all of the substrate is in a diffracting condition, therefore, the observed twins only exist in the β-SiC epilayer. Furthermore, it can be surmised that they were generated at the interface since there is no contrast variation (i.e., shades of gray) in the topograph. Since only light and dark regions of the two different orientations do not overlap.

These boundaries were also observed in plan view TEM as shown in Figure 9. This micrograph indicates that such boundaries (Feature A) are rather high energy as shown by the significant

Figure 7a. XRT micrograph of β-SiC on 6H SiC before rotation.

Figure 7b. XRT micrograph of β-SiC on 6H SiC after 60° rotation around [111] axis of the β- SiC.

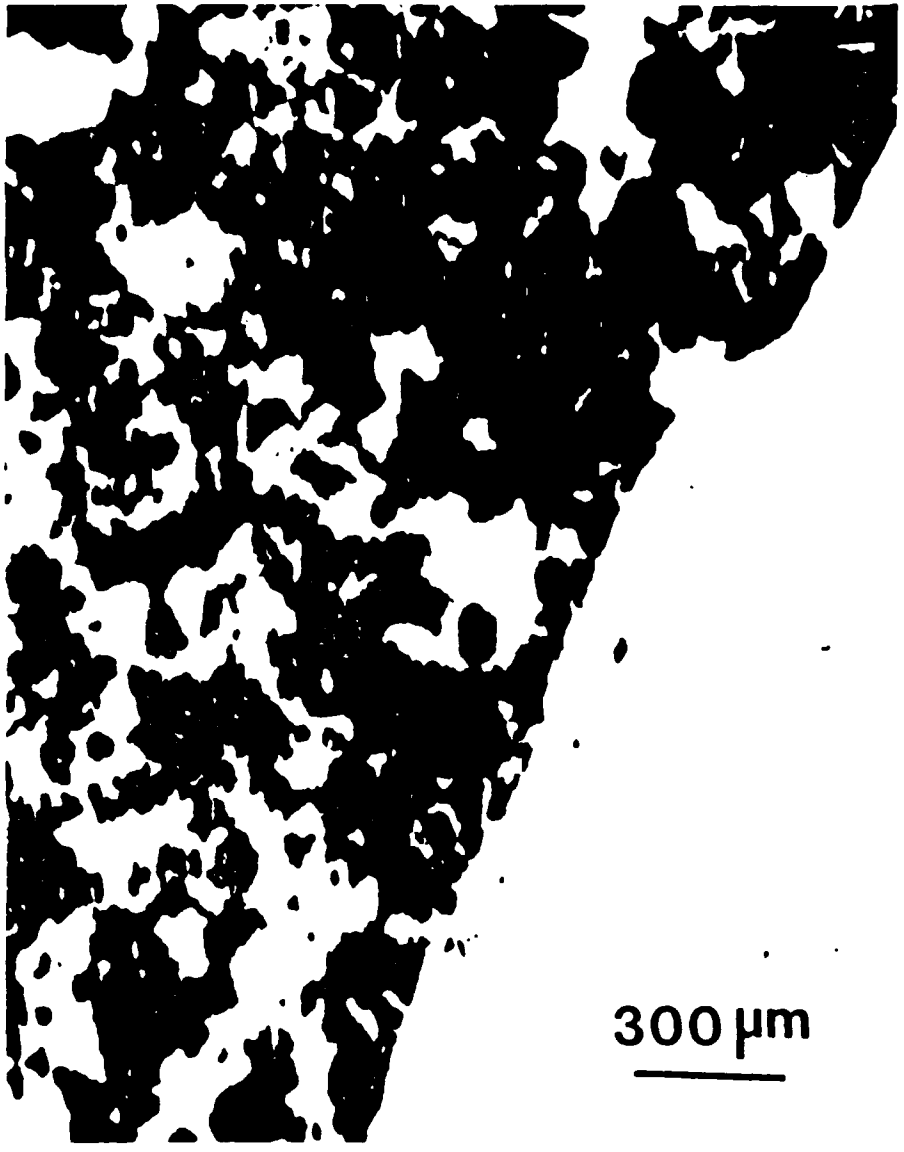


Figure 8a. XRT micrographs from β-SiC thin film.

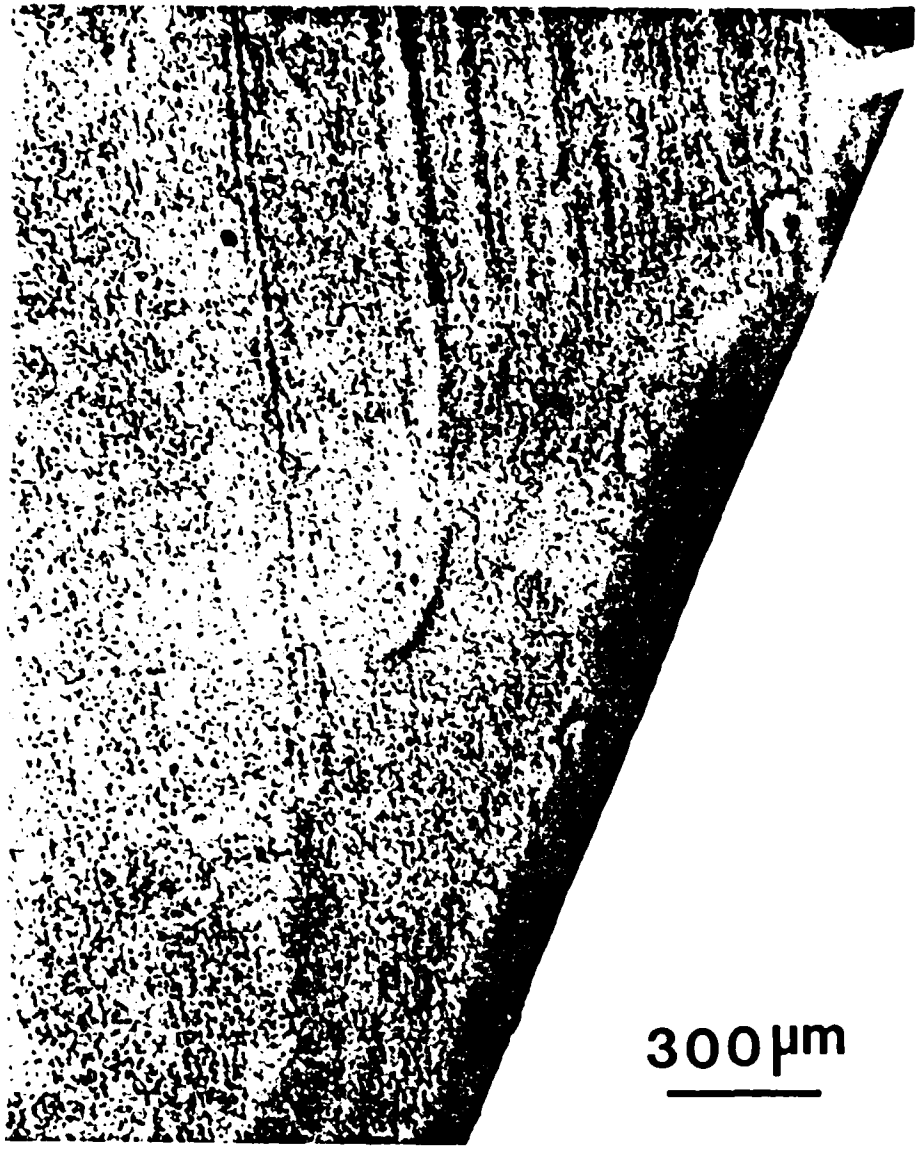


Figure 8b. XRT micrographs from 6H SiC substrate.

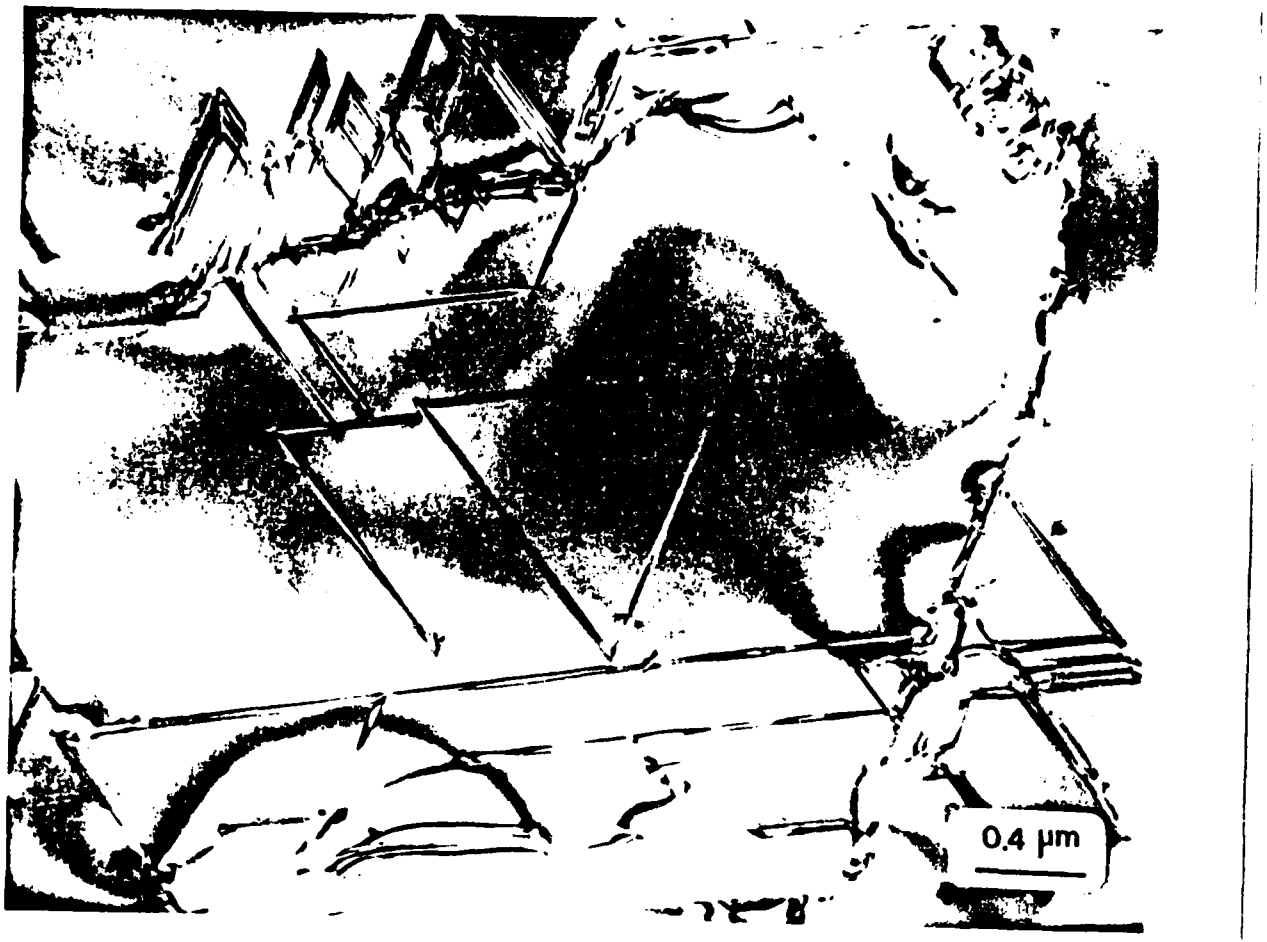


Figure 9. Plan view TEM which shows the stacking faults generated from the DPBs.

strain contrast associated with them. This is further indicated by the numerous stacking faults (Feature B) which appear to be generated at the boundary. The large open area (Feature C) observed in one region of the boundary is probably an artifact of the ion milling necessary for sample preparation. Other defects (Feature D) have also been observed during this TEM examination and will be the topic of a future publication. Similarly, the triangular structures within the domains of the β-SiC films seen in the (331) X-ray topograph in Figure 10 are believed to be another type of defect and are currently under investigation. These features appear to be very similar to those observed in (112) and (110) XRTs of Si films on Si which were verified to be Lomar and Lomar-Cotrell dislocations.[7] However, a thorough Burgers vector analysis must be completed to verify this correlation.

D. Discussion of Observed Boundaries

As previously mentioned, the observed boundaries are a special type of twin boundary. In fact, their properties of (1) separating domains which are related by a 180° twin axis, (2) nucleation at the interface and (3) relatively high energy, define these boundaries as "Double Positioning Boundaries" (DPBs). They have been observed in films of Cu, Au, Pd and deposits of lead chalcogenides formed on substrates such as mica and MoS but have not previously been identified in SiC. DPBs are so-named because they are caused by the existance of two equivalent sites on the substrate surface as discussed in more detail below using the model of M. H. Jacobs and M. J. Stowell[9].

DPBs frequently occur when an fcc deposit is grown in a (111) orientation on a (111) surface or on the basal plane of a hexagonal crystal since there are two types of possible stacking sequences, both of which have close-packed directions aligned in the interface. This is illustrated in Figure 11(a), which indicates that on the 6H SiC (0001) Si face there are two equivalent types of sites on which carbon atoms can locate. Hence, two types of nuclei orientations can be formed on the surface which are rotated 60° relative to each other. The boundary formed where such nuclei grow together is termed a DPB.

A schematic cross sectional view of a DPB and the stacking sequences in the adjacent domains are shown in Figure 11(b). In order to describe the stacking sequences in the two types of domains, (111) layers in the face centered cubic β-SiC lattice are denoted abcabc. . . etc. where a, b and c represent Si-C pairs since a pair of Si-C atoms can be viewed as a lattice point in the fcc structure. In Figure 11(b), the letter A represents the final layer of the substrate which is 6H SiC in the present research. On the left side, the closest packed layers are stacked Abcabc . . ., while on the right side, they are stacked Acbacb . . . The small characters stand for the grown β-SiC layers. The domains with two types of stacking sequences nucleate side by side and then grow together to form the DPB. Although every third plane of Si-C pairs has the potential to form a perfect bond across this interface, the other planes can not. Therefore, the atomic structure is generally disordered at this boundary which causes its internal energy to be rather high; the free energy of an incoherent twin boundary[10] is considered to be 2/3 that of a high-angle grain boundary. This high energy was evidenced by the optical and transmission electron microscopy as discussed in the

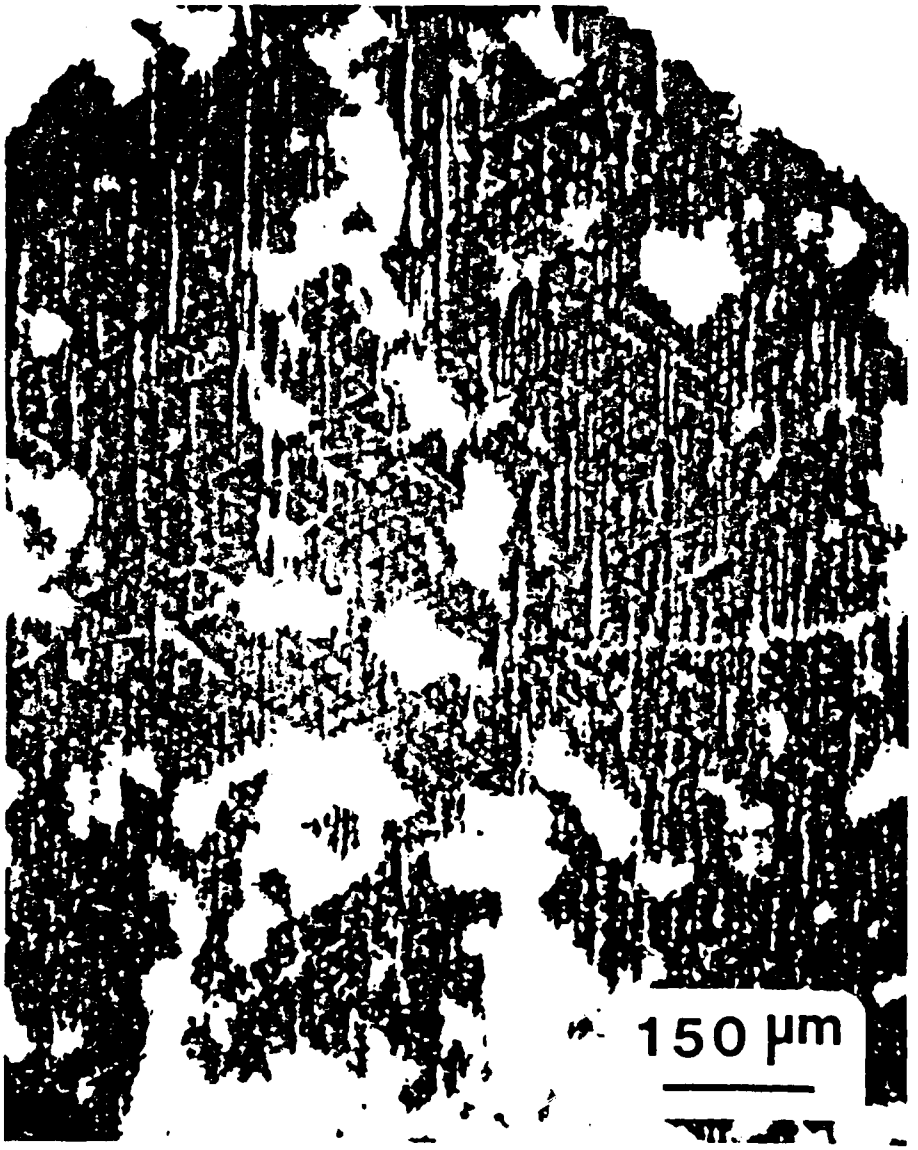
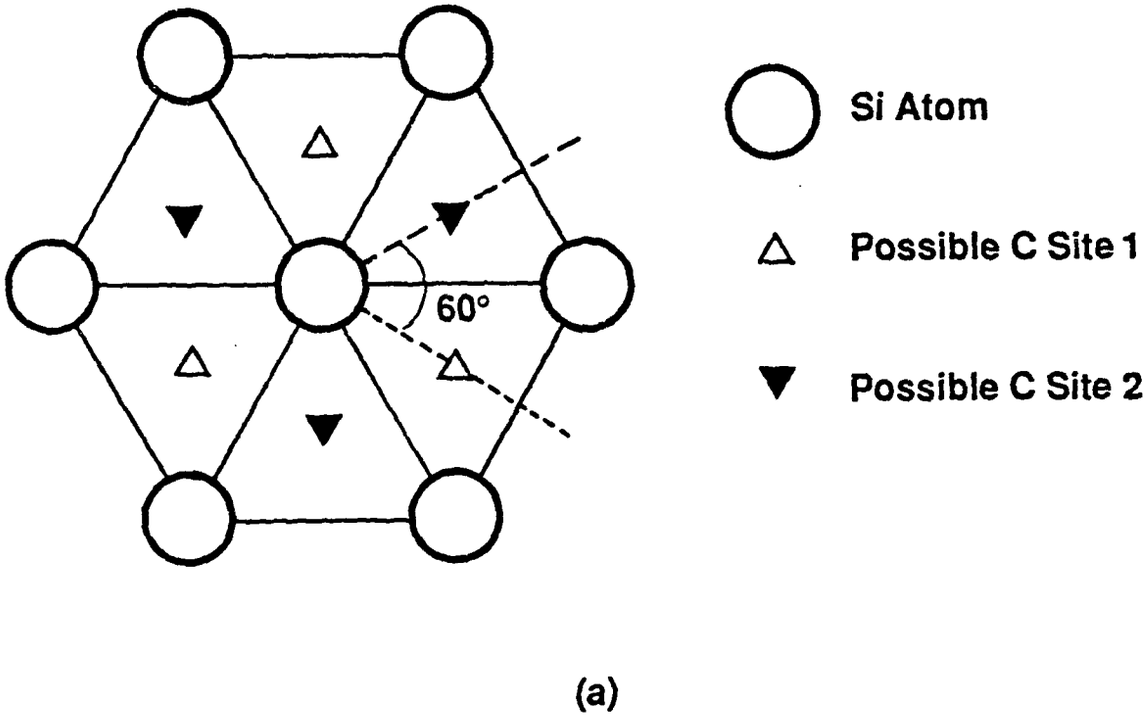


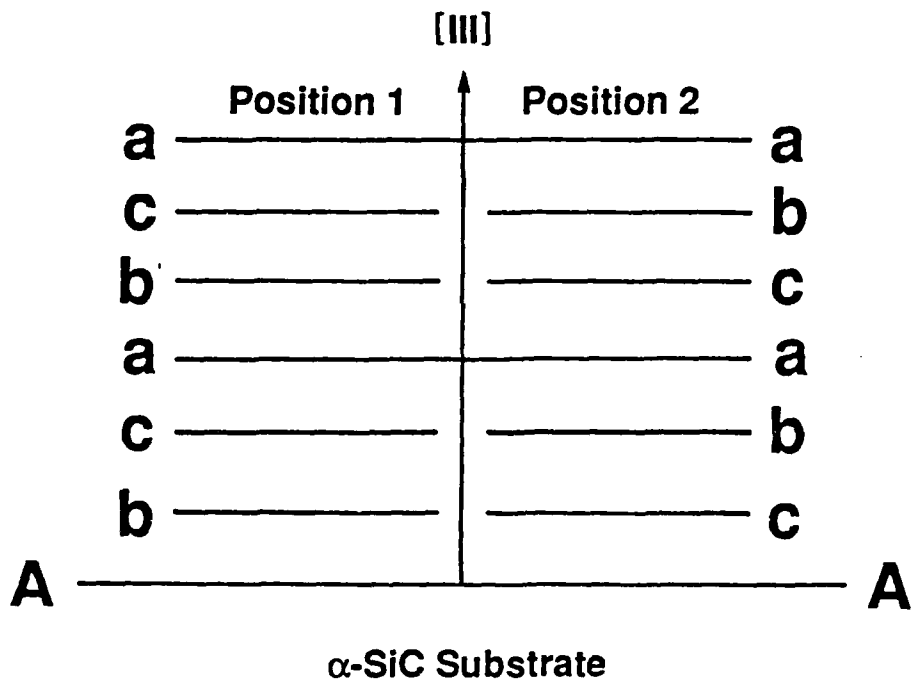
Figure 10. XRT of triangular defects in the β-SiC thin film.

DOUBLE POSITIONING BOUNDARIES IN β-SiC EPITAXIAL FILMS



(a)

Figure 11a. Schematics of explanation for the formation of DPBs: (a) two equivalent sites on the Si face of a 6H SiC substrate.



(b)

Figure 11b. Schematics of explanation for formation of DPBs: (b) two closest stacking sequences for the two different positions.

previous section. It should be noted that DPBs in certain materials, can also contain low energy coherent segments in addition to the incoherent, high energy boundaries described here.[8] Such segments are similar to the more common high energy segments except they lie in (111) planes. None of these coherent DPB segments have been observed to date in SiC.

Conclusions

The β-SiC thin film have been studied via XRT, X-ray rocking curve analysis and plan view TEM. The lattice misfit between the β-SiC epilayer and the 6H SiC substrate was calculated from the rocking curve data. DPBs were found in the β-SiC epilayer which were caused by simultaneous nucleation of the film in different sites rotated from each other by 60°. The as grown surface morphology shows a pattern which exactly correlates with the DPBs as confirmed by comparison of the surface morphology with the XRT. Further work is necessary to analyze the other types of defects observed in the β-SiC epilayers.

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IV. 6H–SiC Films on Off-Axis 6H SiC Substrates

A. Introduction

Beta-SiC is usually considered more desirable than α-SiC for most electronic applications since its electron mobility is postulated to be higher than that of α-SiC over the temperature range of 300 to 1000 K.[1] Furthermore, the growth temperatures of β-SiC are generally lower than those of α forms for various types of growth (i.e., CVD, sublimation, etc.). However, the difficulties in the growth of high quality β-SiC thin films do not allow the electron mobility to attain these postulated values. This is believed to be due to the numerous defects present in β-SiC films, especially those grown on Si substrates. Dislocations, stacking faults and antiphase domain boundaries (APBs) are generated from the β-SiC/Si interface and extend from the interface to approximately 3 μm into the bulk film. In fact, many even propagate up to the as grown surface.[4,5] Even with α-SiC substrates are utilized for the growth of β-SiC, significant concentrations of defects persist in the form of Double Positioning Boundaries (DPBs) and stacking faults.[6] Attempts to eliminate such boundaries in β-SiC films by utilizing off-axis α-SiC substrates led to the growth of 6H SiC as discussed herein.

The growth of 6H-SiC on 6H-SiC substrates via CVD has been reported since the late 1960's. Several papers reported the growth of 6H-SiC on 6H-SiC {0001} in the temperature range of 1773–2023 K[7–9] but a mosaic morphology was observed on the as grown surface. The growth of 6H-SiC films on 6H-SiC in the temperature range of 1593–1663 K was also reported,[11] in which case, the growth direction was perpendicular to the [0001] axis. More recently, Kong et al,[6] and Kuroda et al[12] reported the growth of 6H-SiC on off-axis 6H-SiC substrates. In the later study, a thorough structural examination was not attempted and although certain electrical properties were evaluated and improvements over β-SiC films were observed, further significant improvements have been achieved in the present work. In the former case, although DPBs were reported to have been eliminated, results were preliminary and thorough characterization of the films had not yet been conducted. The present research is a continuation of this study and provides details of a variety of analyses of these films. Both XTEM and plan view TEM were employed to examine the epilayer/substrate interface as well as the bulk 6H-SiC thin film. The relationship between the surface morphology and substrate misorientation was also investigated. The electrical properties, including current-voltage characteristic of Au Schottky barrier diodes, conductivity type and active carrier concentration, were measured to evaluate the electrical quality of the grown films.

B. Experimental Procedures

High purity, defect-free bulk 6H-SiC substrates are not generally available, although recent research in this area appears promising. Therefore, black, industrial 6H SiC {0001} wafers obtained at random from an Acheson furnace were employed in the present research to determine the

feasibility of utilizing such material as a substrate for the CVD growth of SiC. Since 6H SiC is a polar material, {0001} wafers can terminate in either a Si layer (0001) or a C layer (000$\bar{1}$) and a thin crystal with two parallel, smooth surfaces will contain one Si face and one C face opposite to each other. However, the Acheson derived crystals generally contain only one reasonably flat face which is usually, but not always, Si. They usually also contain small (1$\bar{1}$00) facets which allow the determination of the crystal orientation. To prepare these substrates, each was first lapped 3° off of <0001> towards certain orientations (<11$\bar{2}$0> or <1100>) with a set of beveling tools. Secondly, the lapped side was mounted onto a flat plate to lap the other side to obtain a substrate with two parallel surfaces. The lapped wafer was then polished down to 0.1 μm diamond paste. Each 6H SiC substrate was then preoxidized at 1473 K in a flowing dry oxygen atmosphere for 1.5 h to oxidize approximately 50 nm of the polished surface in order to remove the subsurface damage caused by the mechanical polishing. Furthermore, by estimating oxide thicknesses, the polarity of the substrate was determined since the C face oxidizes more rapidly than the Si face. Following this procedure, four kinds of substrates were prepared and used in this research. They are 6H SiC Si (0001) face and C (000$\bar{1}$) face 3° off towards [1$\bar{1}$$\bar{2}$] and [1$\bar{1}$00]. The oxide layer on each substrate was removed with a HF acid solution immediately prior to loading on to a SiC-coated graphite susceptor utilized to hold the samples during growth. The cold wall, vertical barrel-type, rf-heated system which has been described in previous ONR reports was used for the deposition. It was evaluated to 10^{-5} Torr before growth to remove air and moisture. A detailed description of the CVD system is given in Ref. (13).

The substrates were initially heated at 1773K for 600 s in 1 atm of flowing H_2 (3000 sccm) to remove the native oxide on the SiC surface and to clean the surface of certain other impurities. The reactive gases SiH_4 and C_2H_4 were subsequently introduced into the H_2 stream to allow SiC deposition under the same temperature and total pressure. The ratio of the sum of the flow rates (sccm) of SiH_4 and C_2H_4 to the flow rate (sccm) of H_2 was 1:3000. The SiH_4/C_2H_4 flow rate ratio was 2. After desired growth period, the rf generator was shut down to allow the susceptor to naturally cool down to room temperature. The growth period for this research was approximately 3 hours which yielded a film thickness approximately 3 μm.

The surface morphologies of the as grown SiC thin films were evaluated using a Nomarski phase contrast optical microscope. The thin film with the smoothest surface was then prepared to be examined by cross-sectional transmission electron microscopy (XTEM) and plan view TEM coupled with transmission electron diffraction (TED). For the plan view TEM examination, samples were lapped from the substrate side to approximately 2.5 mils. They were then dimpled to about 1 mil. Finally, Ar^+ ion milling was employed to thin the sample from both sides until a small hole was observed. For the XTEM samples, similar preparation procedures were applied perpendicular to the plan of the film after sandwiching the as grown surfaces of two samples together utilizing epoxy. An Hitachi H-800 TEM was used in the present research.

For the electrical measurements of the films after growth, the sample surface must be very clean in order to eliminate the surface leakage. Therefore, the as grown thin films were oxidized and etched under the same conditions as previously mentioned to remove the top 50 nm of the as

grown layer. The carrier type and concentration in the films were measured using a Hewlett Packard 4145A semiconductor parameter analyzer and a LEI Model 2019 Miller Feedback Profiler, respectively, coupled with a mercury probe. Electrical properties of the films were further evaluated by a 2000Å thick layer of Au was thermally evaporated onto the entire surface of the thin film just after stripping the thermal oxide layer. Conventional photolithography techniques were applied to fabricate Au Schottky contact dots which were 100 μm in diameter These dots were surrounded by a large area Au contact which was used as an ohmic contact for this study.

C. Results

Utilizing the growth conditions and substrates previously discussed, 6H α-SiC films were obtained on all kinds of substrates except the substrate tilted 3° off [0001] towards [1$\bar{1}$00], in which case, a mixture of β-SiC and 6H α-SiC was obtained. This result is somewhat unusual because β-SiC is expected to be more stable at the growth temperature employed, although, when the growth mechanism is considered (see Discussion section), it is not surprising. Furthermore, these 6H SiC films were seen to be of very high quality under certain conditions. Therefore, analyses were undertaken utilizing a variety of techniques to more thoroughly understand these films as discussed in the following subsections entitled; (1) surface morphology; (2) TEM analyses; (3) electrical properties. Speculation is also given as to the reasons for certain observations in the following Discussion section.

(1) Surface Morphology

Fine growth steps and some pyramidal growth patterns were observed on the film grown on the Si face of the off-axis 6H SiC substrate while a skin-like pattern was observed on the surface of the film on the C (000$\bar{1}$) face of the 6H SiC substrate. In the cases of growth on the (0001) and (000$\bar{1}$) faces 3° off towards [11$\bar{2}$0] the as-grown surfaces are very smooth. The film on C (000$\bar{1}$) face 3° off towards [11$\bar{2}$0] had fewer features (i.e., smoother surfaces) than those grown on a Si face with the same tilting orientation. In fact, many small elongated pyramidal features in groups were observed in the films on the Si face. The origin of these features is currently not well understood but they indicate that pyramidal vs lateral growth occurred in local regions of the film. It is worthwhile to compare the surface morphology of these 6H SiC films, especially those grown on the off-axis substrates towards [11$\bar{2}$0] with β-SiC grown previously by CVD. Compared with the as grown surface morphologies of the β-SiC thin films grown on exact Si (100), on off-axis Si (100) and on natural 6H SiC (0001) substrates, the surfaces of the films on the off-axis 6H SiC substrates are much smoother.

(2) TEM Analyses

TEM analyses were performed on the as grown 6H SiC films grown on 3° off 6H SiC C (000$\bar{1}$) face towards [11$\bar{2}$0] direction because such films possess the smoothest surfaces. The microstructure of the epilayer/substrate interface region was characterized using XTEM in conjunction with TED. Diffraction patterns obtained from the epilayer and substrate show identical reflections characteristic of the 6H SiC [11$\bar{2}$0] pole. Lattice fringes could be seen in both the epi-

layer and substrate. Lattice fringes, which were traces of (0001) planes, could be seen to cross from the substrate into the epilayer without distortions. The angle between the interface and the lattice fringes was approximately 3° as expected due to the off axis substrate preparation. The different contrast between the epilayer and the substrate which allowed them to be distinguished from one another is believed to be caused by the high impurity level in the substrate, mainly, aluminum ($1–10 \times 10^{19}/cm^3$) and nitrogen ($1–10 \times 10^{18}/cm^3$) as determined by secondary ion mass spectroscopy. No line or planer defects could be seen at the interface. In fact, few defects were observed in the entire XTEM sample. In order to examine a larger area of the bulk 6H SiC thin film, plan view TEM was used. Contrary to the growth of SiC on conventional (i.e., "on-axis") 6H SiC substrates, no DPBs or triangular stacking faults and their modifications were observed. Therefore, both XTEM and plan view TEM verified that a high quality, monocrystalline 6H SiC had been grown on the 6H SiC substrate.

(3) Electrical Properties

The concentration of active carriers and the distribution of these carriers as a function of depth in the α-SiC films in this study were measured using a differential C-V method as previously discussed. The conductivity of the unintentionally doped 6H SiC thin films was always found to be n-type just as the β-SiC films grown on Si (100), off-axis Si (100) and 6H SiC {0001} substrates. The carrier concentration was in the range of $1–10 \times 10^{16}/cm^3$. At an electrical potential of 42 V, the leakage current was only 0.1 μA, whereas the leakage current exceeds the allowed value for the instrument (100 μA) at an applied voltage of 4–5 V for a typical β-SiC film grown on 6H SiC (0001) or on exact Si (100) substrates and 10 V for a β-SiC film grown on an off-axis Si (100) substrate. Therefore, the leakage current has been greatly improved in these 6H SiC thin films, however, the value of the carrier concentration has not been significantly reduced. The origin of the unintentional dopants has been reported to be nitrogen,[14] however, before a final conclusion can be drawn, more analysis is necessary.

Au Schottky barrier diodes were fabricated on an unintentionally doped n-type 6H SiC film grown on a 6H SiC C (000$\bar{1}$) substrate 3° off towards [1$\bar{2}$0]. The epilayer was about 3 μm thick with a carrier concentration of $7 \times 10^{16}/cm^3$. At a reverse bias of 55 V, the leakage current was 2.5 nA ($3.2 \times 10^{-5} A/cm^2$) which is two orders of magnitude lower than previously reported value for α-SiC on α-SiC at a reverse bias of 40 V.[12] When the reverse bias was increased to 65 V, the leakage current increased to 30 nA ($3.8 \times 10^{-4} A/cm^2$). Compared with Au Schottky barrier diodes made on β-SiC films grown on 6H SiC (0001) substrate, the leakage current was greatly reduced.

The forward bias LogI vs V curve for the Au Schottky diode was also evaluated. The ideality factor, n, was determined to be 2.1 from the slope of the linear part of the plot. The saturation current, J_S, obtained from the intersection of the straight line portion of this plot with the current axis was $1.53 \times 10^{-11} A/cm^2$. Generally, when n = 2, recombination current presumably dominates the forward conduction. However, as is the case with insulators and wide bandgap semiconductors, conduction in SiC occurs primarily by space-charge-limited current (SCLC) flow.[15] Furthermore, in junction diodes fabricated in β-SiC, the SCLC is dominated by shallow and deep trapping effects.[16] Therefore, a detailed analysis of LogI–LogV characteristics of the

present diodes is necessary and is presently being carried out in order to understand the conduction mechanism and trapping effects involved.

D. Discussion

It is useful to discuss the large differences in the surface morphologies of the films grown on the 6H SiC {0001} substrates tilted towards [11$\bar{2}$0] vs. [1$\bar{1}$00] caused by the different atomic arrangements of the different misorientations. In both cases the "off-axis" preparation of the substrate surface (as described earlier) causes a series of steps and ledges to be formed to accommodate the misorientation. The average spacing of the steps are largely determined by the degree of misorientation. This stepped surface can also be thought of as a very high index plane. Prior to the CVD process these substrates have a mirror finish because the steps are microscopic. No roughness is visible to the naked eye or under an optical microscope. However, during CVD, a step bunching process can occur which increases the average height and separation of surface steps until they are readily visible under an optical microscope. This step bunching occurs for two primary reasons. First, the lateral growth velocity of a step is inversely proportional to its height.[17] Therefore, if steps are nonuniform on a surface then those of smaller height will "overtake" larger steps creating step bunching and therefore increasing surface roughness. Step bunching can also be caused by the nonuniform adsorption of impurities, thus slowing the lateral growth of some steps.[18] It is this latter mechanism which is believed to be dominant in the present case as discussed below.

As previously discussed, the films grown on SiC (0001) substrates prepared off-axis in the [1$\bar{1}$00] direction were significantly rougher than those grown on [11$\bar{2}$0] direction off-axis substrates. This can be explained by examining the orientation of the steps created in these two different cases. Steps on the [1$\bar{1}$00] off-axis substrates are parallel to the closest packed direction in the (0001) surface; the [11$\bar{2}$0] direction.[18] Thus, these steps are relatively smooth low energy steps and contain relatively few incorporation sites for easy lateral growth. Consequently, growth is slow and is easily poisoned by the adsorption of impurity atoms. This causes step bunching and a rough surface. On the other hand, steps on the [11$\bar{2}$0] off-axis substrates are parallel to [1$\bar{1}$00] direction on the substrate surface. This is not a close packed direction and therefore the steps contain much more kinks which can act as incorporation sites for lateral growth. Therefore, the actual surface area and the lateral growth rate of these steps is increased over the case of a step parallel to the closest packed direction. Consequently, the effect of impurity atoms is minimized, resulting in a relatively smooth as grown surface.

It is also worthwhile to discuss the reason that 6H SiC films were obtained in this research at temperatures where β-SiC is generally more stable as well as why DPBs were not obtained in these 6H films. Both of these phenomena can be directly attributed to the nucleation phase of the film on the off-axis substrates. As is well known, DPBs are caused by nucleation on two equivalent sites on the substrate surface (for example, utilizing ABC stacking nomenclature, B sites or C sites can be the nucleation sites on an A type substrate surface).[19] As these nuclei grow together, boundaries form between them which are referred to as DPBs. However, if the natural (0001) plane is

lapped a few degrees off from the exact ⟨0001⟩ direction, many steps and kinks are created on the surface. Initial film growth is then controlled by these kink and step sites rather than the growth of the two dimensional nuclei. Therefore, if surface diffusion is sufficient and the steps are sufficiently close together, the atoms incorporate along these edges. Since each edge defines a single type of site (i.e., A B or C, depending on where in the stacking sequence the step is located) domains separated by DPBs are not able to form. However, due to this step nucleation, β-SiC is not formed even at relatively low growth temperatures where it is usually favoured. Rather a thin film with the identical crystal structure as the substrate, i.e., 6H SiC is grown. This is not unexpected since a series of steps defines the stacking sequence of the nucleating film. For example, in a simple hexagonal structure containing single unit cell steps assume an A plane terminates to form a given step. The step above this "A step" will naturally be formed by the termination of a B plane and the next by the termination of a C plane. This sequence will then repeat itself. Therefore, the step nucleation of three consecutive planes will form an ABC stacking sequence and the substrate structure is exactly reproduced. This phenomenon is complicated by the existence of steps with varying heights, however, a similar result is obtained. The substrate structure is reproduced because kink sites where incorporation occurs follow the bulk structure even if the step is of multi-atom height.

E. Conclusions

Monocrystalline 6H SiC thin films with flat, smooth surfaces have been epitaxially grown on 6H SiC {0001} substrate 3° off-axis towards [11$\bar{2}$0]. Using 6H SiC {0001} substrates 3° off-axis towards [1$\bar{1}$00] did not result in a featureless surface. TEM analysis revealed that DPBs were eliminated by using the 3° off C face towards [11$\bar{2}$0] substrates, and that no line and planar defects were generated from the epilayer/substrate interface. In fact, few defects were observed in the entire thin film. The conductivity of the unintentionally doped 6H SiC thin films was always n-type. The active carrier concentration of these films was in the range of 1–10 x $10^{16}/cm^3$ which is similar to that of CVD β-SiC thin films. Au Schottky barrier diodes were fabricated on a 6H SiC film and it was found that the leakage current was extremely small compared with that of the diodes made on CVD grown β-SiC films on various substrates.

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v. Ion Implantation in ß-SiC: Effect of Channeling Direction and Critical Energy for Amorphization

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ABSTRACT

Damage in single crystal β-SiC(100) as a result of ion bombardment has been studied using Rutherford backscattering/channeling and cross-section transmission electron microscopy. Samples were implanted with Al (130 keV) and Si (87 keV) with doses between 4 and 20 x $10^{14}cm^{-2}$ at liquid nitrogen and room temperatures. Backscattering spectra for He^+ channeling as a function of implantation dose were initially obtained in the [110] direction to determine damage accumulation. However, the backscattered yield along this direction was shown to be enhanced as a result of uniaxial implantation-induced strain along [100]. Spectra obtained by channeling along this latter direction were used along with the computer program TRIM to calculate the critical energy for amorphization. The results for amorphization of β-SiC at liquid nitrogen and room temperature are ~ 14.5 eV/atom and ~ 22.5 eV/atom, respectively.

INTRODUCTION

The processing steps leading to the development of selected electronic devices in cubic (beta) silicon carbide (E_g = 2.2 eV) thin films involve ion implantation to introduce electrically active dopants. Recently, this doping method has been successfully utilized in producing p-n junction diodes [1, 2] and metal-oxide-semiconductor field-effect transistors [3] in β-SiC. As is the case with other semiconductors, nuclear scattering events which occur during the deceleration of an implanted atom, results in lattice damage. As the dose of the implanted specie is increased, the near surface region becomes progressively damaged; atomic disorder and eventual amorphization of the structure occurs.

Early work by Hart et al. [4] utilized Rutherford backscattering/channeling (RBS/C) techniques in order to study both disorder production in monocrystalline, hexagonal 6H α-SiC (E_g = 2.8 eV) by ion implantation and the subsequent thermal annealing of that damage. Williams et al. [5] have previously considered structural alteration in monocrystalline (0001) α-SiC as a result of Cr and N implantation. In each case the channeling direction was taken along [0001]. The latter authors have made direct comparisons of the theoretical damage profiles calculated using the computer codes E-DEP-1 [6] and TRIM [7] with those determined by RBS/C on experimentally implanted SiC samples. It was determined that the critical energy density for amorphization, E_c, in their material was between 10 and 20 eV/atom at room temperature (RT). Edmond et al. [8] found that a critical energy of ~ 16 eV/atom was required for RT amorphization of β-SiC via implantation of Al and P. In their research, the channeling direction was taken along [110] which possesses the widest channels in the FCC zincblende structure of β-SiC. However, experimental damage profiles obtained by channeling in this axis, did not correlate well with theoretical predictions.

The first objective of this research is to compare RBS/C spectra as a function of channeling direction and to establish a hypothesis regarding the differences observed. This research was supplemented with the implementation of cross-section transmission electron microscopy (XTEM). The second objective in our investigation is to employ RBS/C and Monte Carlo computer simulations (TRIM) together with the critical energy density model [9] for implantation-induced damage production in order to quantify the disordering process during ion implantation in β-SiC at RT and liquid nitrogen (LN) temperatures.

EXPERIMENTAL

Thin films of monocrystalline β-SiC were epitaxially grown in-house on (100) silicon wafers via chemical vapor deposition [10]. Each sample was then mechanically polished, oxidized, and etched in HF in order to obtain a clean, undamaged and smooth surface. After mounting in high vacuum, samples were implanted at RT and LN temperature with either Si or Al at energies of 87 keV and 130 keV, respectively. Doses on the Si-implanted samples ranged from 1.7×10^{14} /cm^2 to 2.0×10^{15} /cm^2 and those for Al from 2.0×10^{14} /cm^2 to 2.0×10^{15} /cm^2. It was within these limits that the samples underwent a crystalline to amorphous transition. Aluminum is used as a p-type dopant in β-SiC whereas Si was employed as a preamorphizing, electrically neutral species. The implants were made at an incident angle 7° off normal to avoid channeling effects.

Following implantation, backscattering analyses of the samples was obtained using 2.0 MeV ^{4}He ions incident along [110], [111], and [100]. The dosimetry was stepwise increased and additional ion scattering analyses made in order to measure the incremental increase in lattice damage as a function of implantation dose.

Lattice damage in the surface implanted regions was visually evaluated using XTEM. The procedure for XTEM preparation of the β-SiC samples in this research is discussed in Ref. 11. High resolution lattice fringe images and convergent beam electron diffraction (CBED) patterns of the damaged regions were also obtained.

Theoretical damage energy deposition profiles have been obtained for implantation of both species using the Monte Carlo simulation program TRIM [7, 12]. these calculations were executed using a threshold displacement energy of 16 eV for SiC [8]. Amorphous layer depths from RBS/C results were directly compared to the TRIM plots to obtain E_c at both LN and RT.

RESULTS AND DISCUSSION

A. RBS/C and XTEM Analysis

Rutherford backscattering spectra taken as a function of ion dose for 130 keV Al-implanted β-SiC at LN temperature, are shown in Fig. 1. Also shown is a spectrum from an unimplanted sample and a random spectrum obtained by varying the direction of incidence. The incident beam was aligned with the bulk SiC [110] axis for these spectra. Chi min, defined as the ratio of the near-surface aligned to near-surface

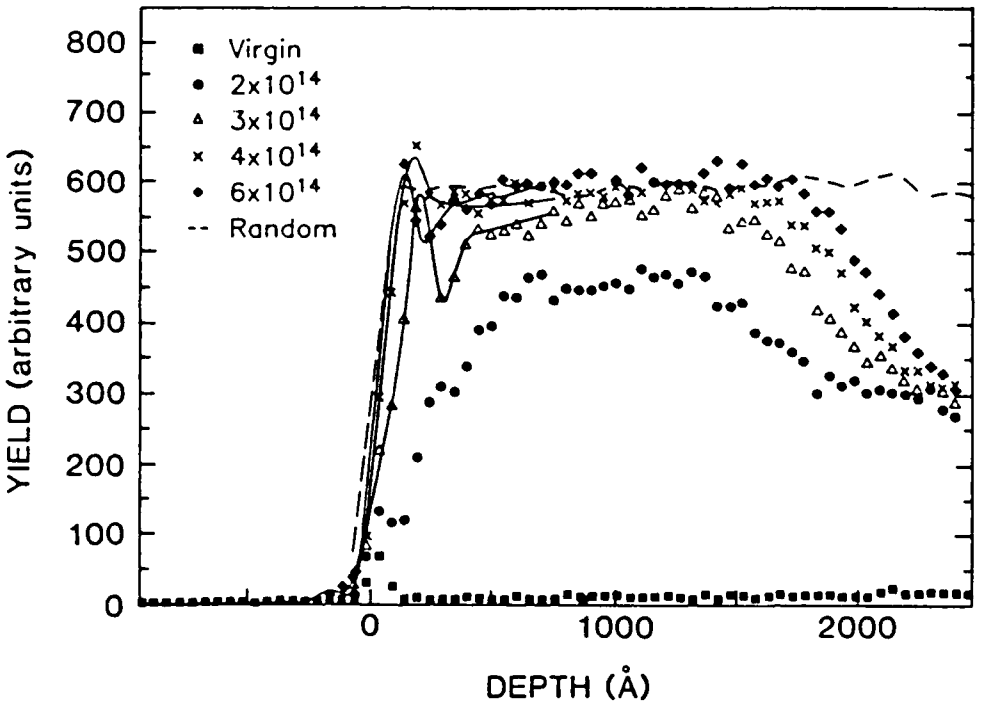


Fig. 1. 2.0 MeV He^+ backscattering spectra from β-SiC for different implant doses of 130 keV Al. The depth scale is referenced with respect to Si at the surface. Scattering from the C in the substrate is not shown.

random yields, calculated for the virgin spectrum, is 0.013, which is excellent for channeling, but approximately a factor of 3 higher than theoretically predicted [13]. In the region of greatest damage accumulation, the lowest dosed spectrum has a characteristic flat-topped yield which is less than the yield of the random. At higher

doses the yield reaches the random yield over some buried depth. In all the implanted spectra a near surface peak is seen 15 to 30 nm below the surface. This peak is observed closer to the surface with increasing dose. For some spectra this peak goes above the random level as emphasized by lines drawn through the data. For ion doses greater than 1.0×10^{15} /cm^2 (not shown in the figure) the aligned and random yields are the same throughout the damaged layer and TEM results indicate the sample is amorphous from the surface down. The spectra of Fig. 1 are qualitatively similar to spectra obtained for Al and P implantation at RT [8] as well as P and Si implantation into samples cooled by LN.

RBS spectra obtained by channeling in three low index axes in a sample implanted at LN temperature with 4.0×10^{14} Al/cm^2 are shown in Fig. 2. Alignment along the axes was determined by scanning in the bulk, undamaged material. The spectra have been normalized to a random spectrum obtained for each axis. The two spectra obtained for non-normal incidence, [110] and [111] (45° and 54.73° from normal, respectively), achieve the random yield over a depth interval below the surface, whereas the spectrum taken along the normal [100] axis does not. In addition, the near surface peak is only seen in the spectrum for the [110] axis.

Two unexpected results are seen in these RBS spectra: the near surface peak and the rather flat, less than random yield over a buried depth in the spectra for some doses. From deposited damage energy considerations [8] the distribution of the damage would be expected to show a broad peak. To help understand these results, selected samples were examined via XTEM. Figure 3 shows a series of micrographs taken of the surface region of the sample used to obtain the spectra in Fig. 2. The micrograph of Fig. 3(a) shows three distinct layers: ~ 40 nm crystalline surface, a heavily damaged buried region ~ 100 nm in width (labeled "A" on the micrograph), and the SiC substrate. The micrograph was taken using 2-beam diffracting conditions (g = [200]) near the [001] zone axis. A planar defect runs through the underlying crystalline β-SiC to the buried region, appears to end, and is present again in the crystalline surface; this suggests, upon

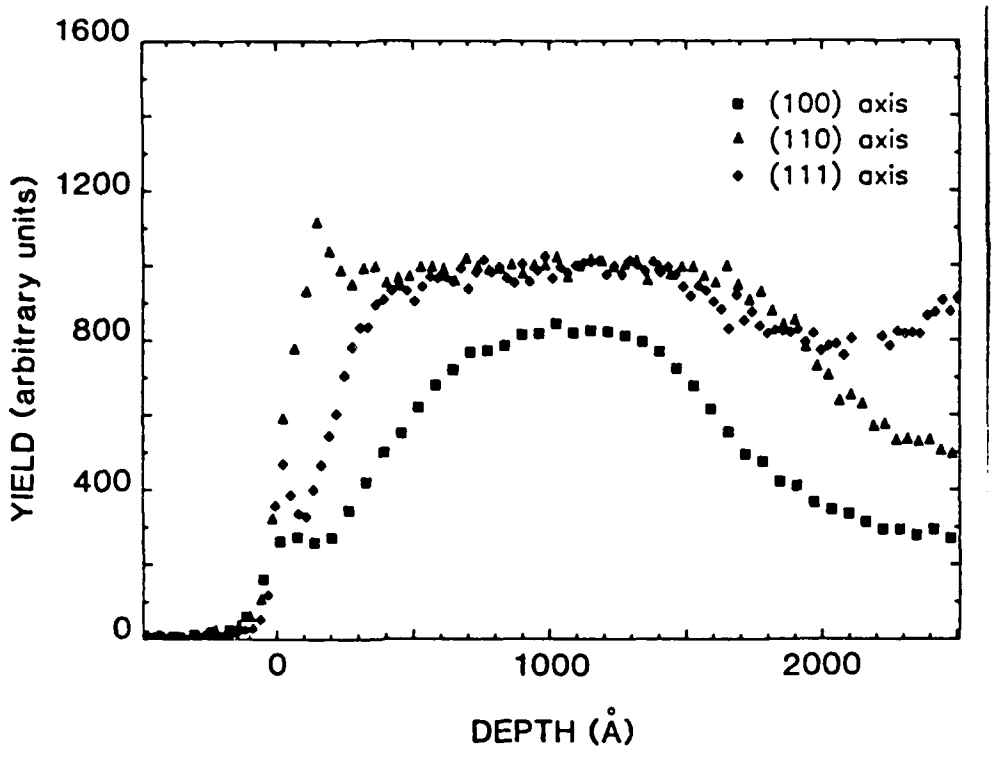


Fig. 2. Comparison of channeling spectra taken along the bulk [100], [110] and [111] axes of a sample implanted at liquid nitrogen temperature with 4.0 x 10^{14} Al/cm^2. Implant energy was 130 keV. Scattering angle was 147° for the [100] and [110] axes and 155° for the [111] axis.

initial examination, that the buried region is amorphous. However, when the sample is tilted to the [011] zone axis, high resolution imaging reveals that this region is actually mostly crystalline with small, isolated amorphous pockets throughout the buried layer, as shown in Figs. 3(b) and 3(c) (Fig. 3(c) is a magnified view of the boxed area in Fig. 3(b)). The (111) lattice fringes are clearly evident in Fig. 3(c); the fringes are continuous throughout the crystalline surface and are also present in the matrix of the buried damaged region, but are not observed in small areas which are amorphous islands (indicated with arrow) below the interface. The crystallinity is clearly present in the buried region. This damaged region corresponds roughly in depth to the region in Fig. 1 in which the corresponding aligned RBS spectrum is flat topped.

Convergent beam electron diffraction patterns, with the crystal aligned at the [001] zone axis, are shown in Fig. 4 for the three regions labeled in Fig. 3, respectively. The

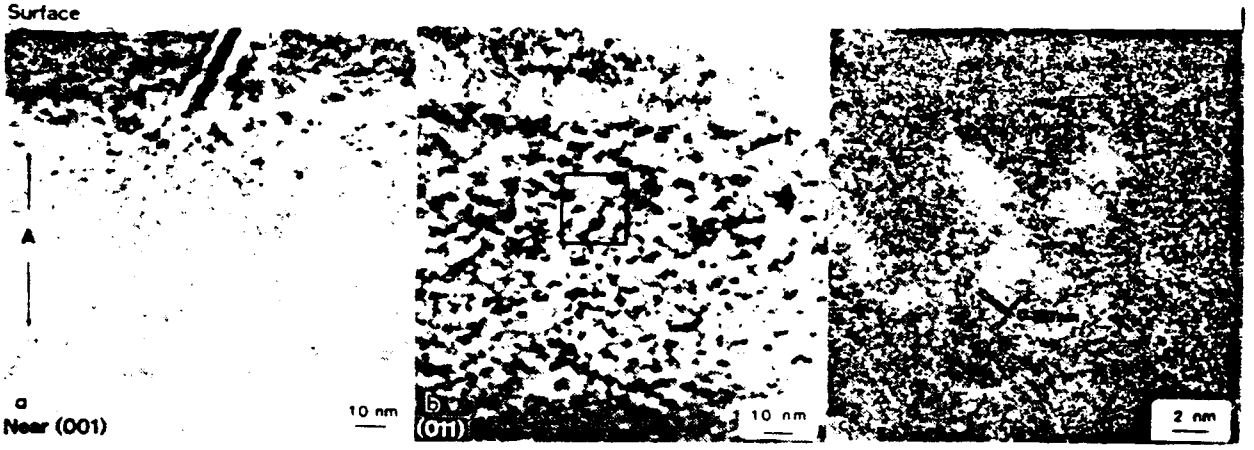


Fig. 3. Cross-section TEM micrographs of a β-SiC sample implanted with 4 x 10^{14} Al/cm^2 at liquid nitrogen temperature (**a**) sample oriented close to [001], (**b**) sample oriented on [011] zone axis, and (**c**) high resolution of boxed region in (**b**). Lattice fringes are from (111) planes (0.251 nm). Arrow shows an amorphous pocket.

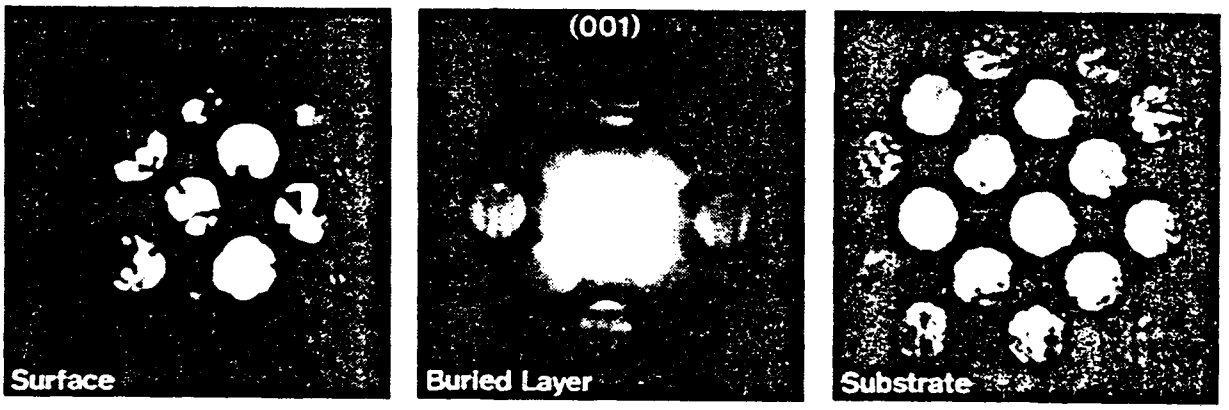


Fig. 4. Convergent beam electron diffraction patterns for [001] zone axis orientation at three depths for same sample used to obtain the micrographs in Fig. 3.

microdiffraction patterns of the top surface and the SiC substrate show complete crystallinity. However, the CBED pattern of the buried layer shows diffuse rings characteristic of amorphous material in addition to the (001) matrix spot pattern. This corresponds well with the results obtained from the high resolution micrograph of Fig. 3(c).

Because the results of Figs. 3 and 4 indicate the surface region is crystalline, attempts were made to find a [110] axis in this layer. Fig. 5 shows an RBS spectrum obtained from a channel found by rotating the sample 0.6° closer to the normal. The tilt

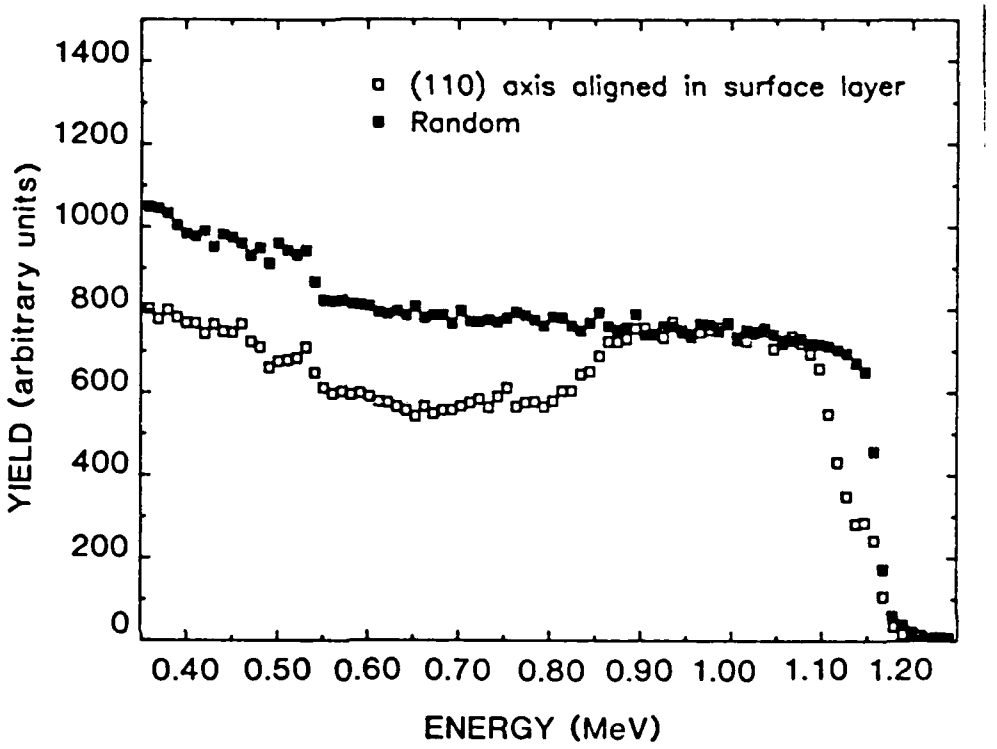


Fig. 5. 2.0 MeV He^+ channeling spectra aligned along [110] in the surface layer. The axis was found by setting an angular scan window only in the top 30 nm of the sample.

angle needed to find the surface layer [110] axis is consistent with a uniform expansion of 2%, although the degree of uniformity of the strain cannot be determined from this data. Note that the peak structure just below the surface is not seen in this spectrum. Since this [110] axis is 0.6° from the axis used to obtain the data in Fig. 1, dechanneling in the bulk SiC is slightly higher, as expected, than when aligned along the bulk [110] axis.

Ion channeling measurements are sensitive to the number and depth distribution of defects; however, the types of defects present are often difficult to determine with this technique [14]. Electron microscopy, on the other hand, can be used to help identify the

microscopic nature of the damage. In the present work, however, no structural damage is identified except for line and planar defects in the as grown samples, that have little effect on the RBS spectra (as evidenced by the excellent channeling in the unimplanted material), and small amorphous pockets below a surface layer. No completely amorphous layer is seen at least for doses up to 4 x 10^{14} /cm^2. Hence, gross structural damage cannot account for the enhanced scattering seen just below the surface in the RBS spectra of Fig. 1 nor the random level scattering yield seen for off-normal channeling. This conclusion is supported by the microdiffraction patterns in Fig. 4, where the well-defined spots are indicative of a crystalline surface layer and a partially crystalline layer below.

Although transmission electron microscopy is not sensitive to point defects, ion channeling can be. The backscattering spectra can be explained, as discussed below, by assuming a lattice strain along the [100] axis induced by point defects. Strain following ion implantation has been reported before [15, 16], although we are not aware of RBS data such as those given in Fig. 1. As demonstrated by the results of Fig. 5, a significant expansion in the surface layer for Al implantation of 4 x 10^{14} /cm^2 is clearly seen.

An incident ion beam aligned along a bulk crystallographic axis in our sample will not be aligned along that axis in the expanded surface layer, except in the case of normal incidence. For ions incident just off a crystallographic axis, the nuclear encounter probability, and hence the backscattering yield, can be increased at a depth approximately equal to a quarter wavelength of the channeling ion trajectory [17], *i.e.*, the depth at which the channeled ions approach the boundary of the channel. This depth is on the order of 20 nm for the conditions employed in this research. This is approximately the same depth at which the peak was experimentally observed (see Fig. 1). The decrease in depth of the peak in this figure at higher doses would indicate an increase in strain with dose, a reasonable expectation. Note that a near surface peak is not seen along the [111] axis. Monte Carlo computer simulations are being initiated to study this peak and to

explain the differences seen for the two axes.

Below the surface layer the lattice is clearly not completely amorphous at any depth following ion implantation of 4.0×10^{14} Al/cm^2, despite the random level scattering yield over a significant depth. Evidence for this is seen both in the lower than random backscattering yield of the [100] axis spectrum and also in the (111) lattice fringes observed in TEM micrographs from this region in [011] oriented samples. However, the random level backscattering yield for off-normal axes, and the contrasting lack of damage structure seen in TEM, except for isolated amorphous pockets, suggests that significant lattice strain resulting from point defects is present in this region as well.

B. Determination of E_c

The appropriate direction for channeling for determination of amorphous layer depths was taken as [100]. The RBS spectra in Fig. 6(a) illustrate the accumulation of damage in β-SiC as a result of 87 keV Si implantation into a sample cooled by LN. Prior to implantation, a virgin aligned and rotating random spectrum were taken as the damage boundary conditions. As can be seen in this figure, damage accumulated in the sample with increasing doses from 1.7×10^{14} /cm^2 until the scattering yield from the damaged region of the aligned spectrum was coincident with the yield from a random spectrum. For the [100] axis in β-SiC, this is indicative of the creation of an amorphous layer. This condition initially occurred at a depth of ~ 55 nm from the sample surface for a dose of 3.5×10^{14} /cm^2. The width of the amorphous region increased with increasing implant dose. At the highest dose measured, 1.0×10^{15} /cm^2 (not shown), a layer amorphous from the surface down to ~ 110 nm resulted.

In order to determine E_c for amorphization, experimental depths over which the Si implant amorphized the material were measured for each implant dose. These are plotted in Fig. 6(b). Also shown in this figure are the theoretical results for amorphization of SiC at LN. The data have been measured from the spectra in Fig. 6(a) by taking the depths at which the yield in the aligned spectra just reached the random value. The

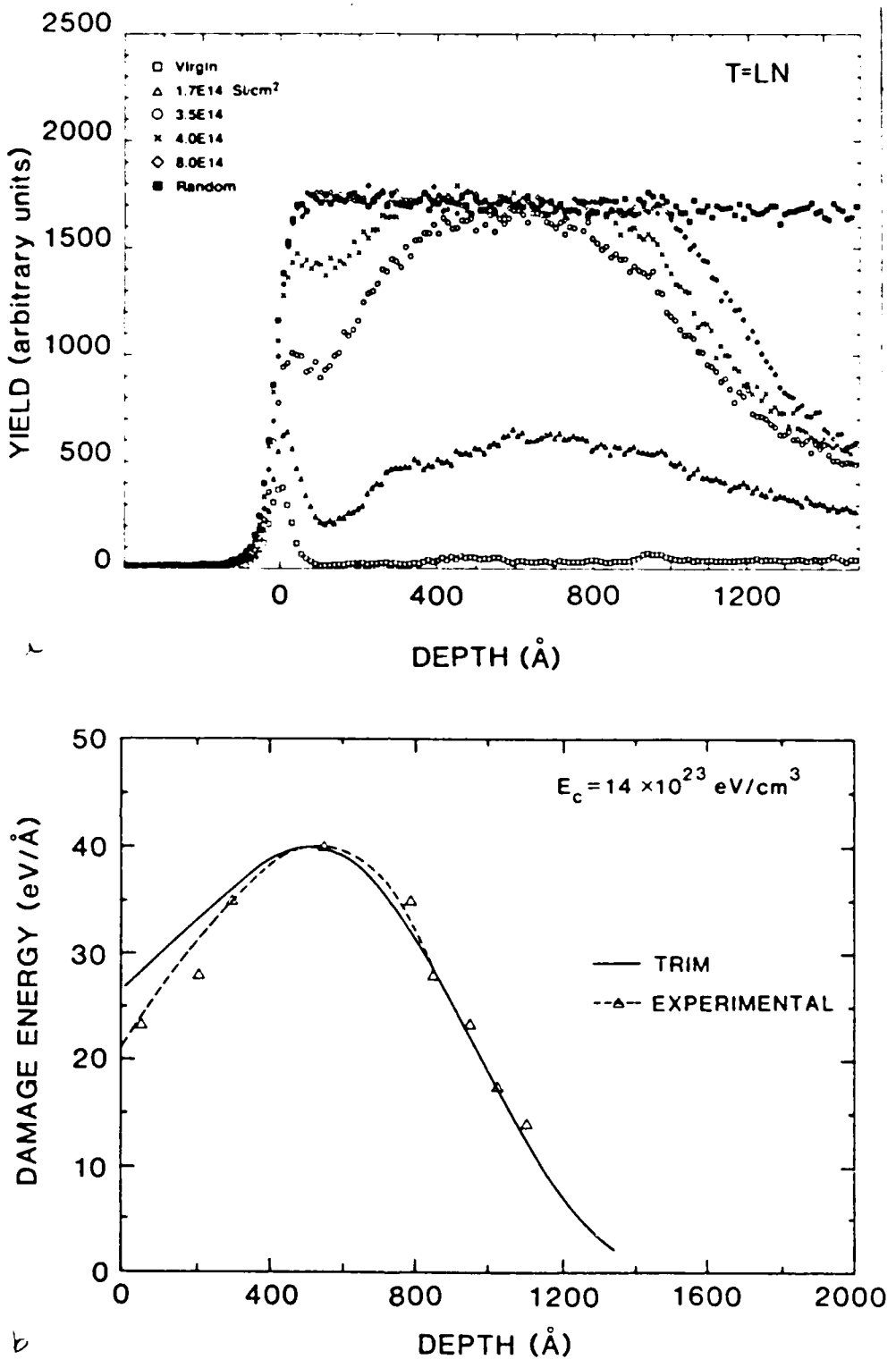


Fig. 6. (a) 2.0 MeV He^+ backscattering spectra for 87 keV LN Si-implanted β-SiC showing the accumulation of damage along [100] with increasing dose and (b) the corresponding comparison between TRIM and experimental damage energy profiles.

uncertainty in these depth values is on the order of the width of the leading edge of the random spectrum [18]. The ordinate represents the energy deposition in eV/Å as determined from TRIM calculations. Amorphous layer depths are plotted in Fig. 6(b) with the corresponding ordinate equivalent to E_c/dose. Best fit results using polynomial regression analyses, indicate an E_c value of ~ 14 x 10^{23} eV/cm^3, or ~ 15 eV/atom for amorphization of SiC cooled by LN.

The dose upon which amorphization occurs (critical dose, D_c) can be emperically obtained by simply taking the ratio of E_c to the maximum damage energy from either the TRIM or experimental damage energy profiles. Under the above conditions D_c = 3.5 x 10^{14} /cm^2 as was observed experimentally in Fig. 6(a). This parameter is a function of the implanted species, implantation energy and implantation temperature

Figure 7(a) shows the RBS spectra for damage accumulation as a result of LN implantation of 130 keV Al in β-SiC. The sample first because amorphous at a dose between 2 x 10^{14} /cm^2 and 4 x 10^{14} /cm^2. From the midpoint of the amorphous region obtained for the 4 x 10^{14} /cm^2 implant, one can approximate the initial depth of amorphization at 104 nm.

Theoretical and experimental damage versus depth profiles for Al implants made at LN temperature are shown in Fig. 7(b). The data were obtained utilizing the same method as for the Si implant described in Fig. 6(b). The critical energy density for amorphization for these conditions was determined to be ~13 x 10^{23} eV/cm^3 or ~ 14 eV/atom. From calculation, D_c = 3.7 x 10^{14} /cm^2. Due to the similarities in atomic masses and implantation energies used in these experiments, the D_c values obtained for Si and Al at LN were very similar. The critical energy density, which is a material property dependent only on temperature, should be constant for these two cases. As seen, values of E_c differed by ~ 1 eV/atom. On the average then, ~ 14.5 eV/atom is required to amorphize SiC under LN conditions.

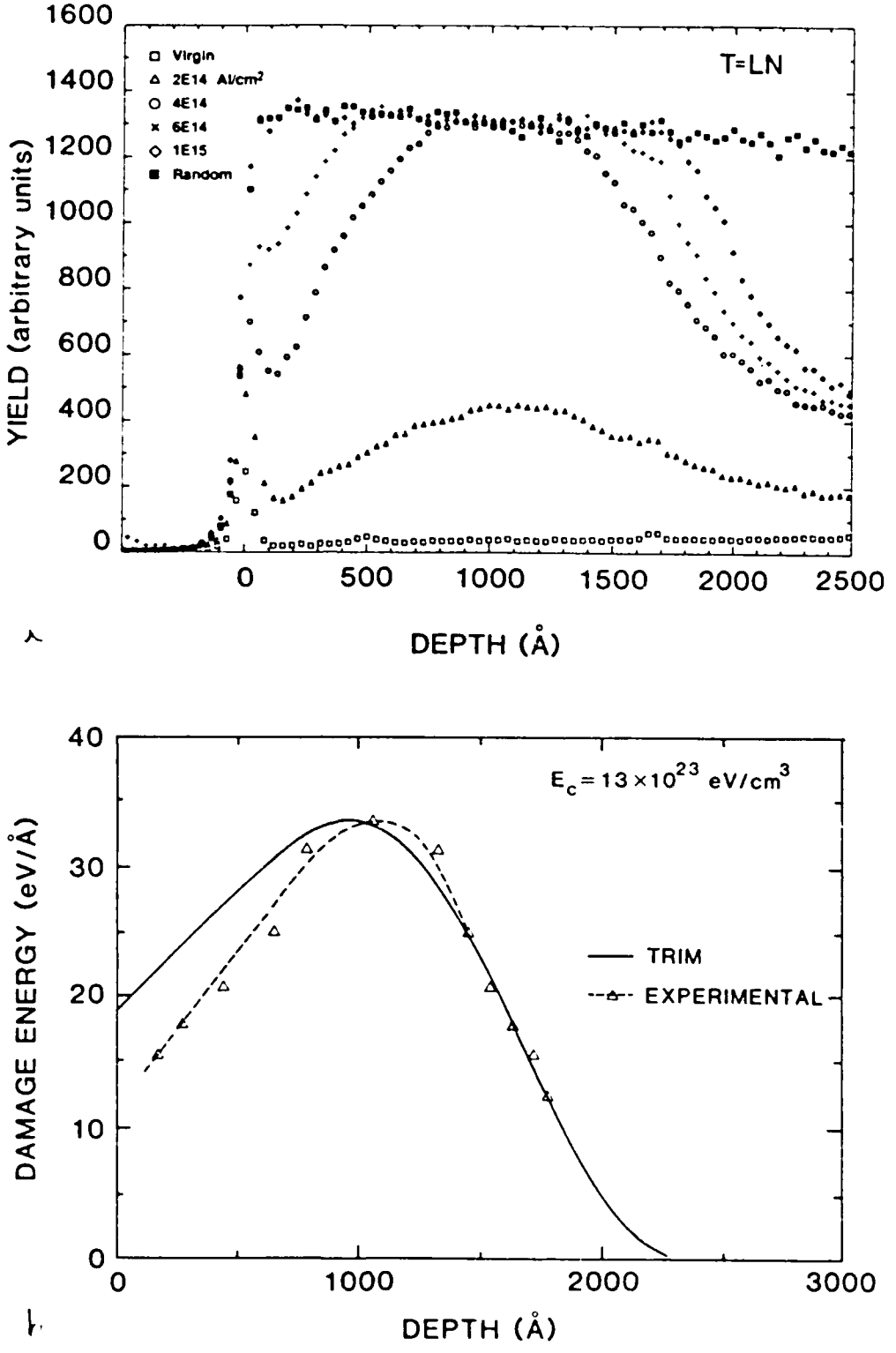


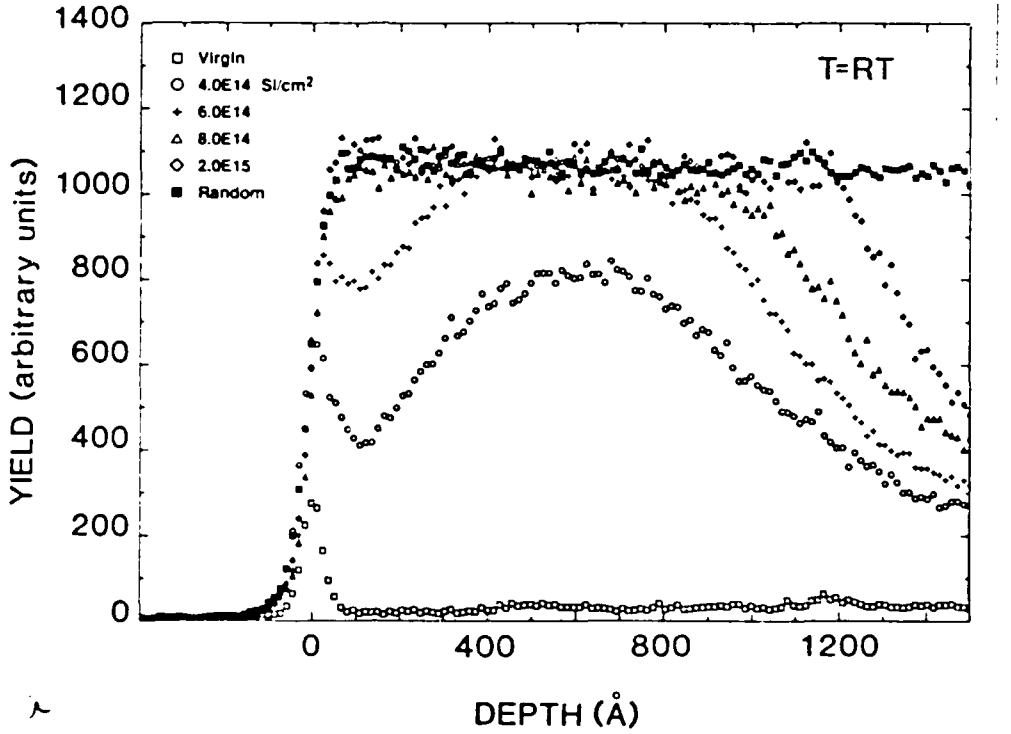
Fig. 7. (a) 2.0 MeV He^+ backscattering spectra for 130 keV LN Al-implanted β-SiC along [100], and (b) the corresponding TRIM and experimental damage energy profiles.

In addition to the above amorphization process, RT amorphization in SiC was considered. Figure 8(a) illustrates the accumulation of damage in this material during RT implantation of 87 keV Si. Clearly, D_c is between 4 x 10^{14} /cm^2 and 6 x 10^{14} /cm^2. Amorphization occurs initially at a depth of ~ 57 nm. The corresponding experimental and theoretical damage energy profiles are shown in Fig. 8(b). In this instance, E_c was determined to be ~ 22 x 10^{23} eV/cm^3 or ~ 24 eV/atom. Additionally, the value of D_c is 5.5 x 10^{14} /cm^2. As expected, both of these values are higher than the results obtained for LN, Si implantation.

Figure 9(a) shows the RBS/C results for 130 keV RT, Al-implanted SiC. The material initially becomes amorphous at ~ 117 nm between doses of 4.0 x 10^{14} /cm^2 and 6.0 x 10^{14} /cm^2. From a comparison of the damage energy profiles shown in Fig. 9(b), E_c was determined to be ~ 19 x 10^{23} eV/cm^3 or ~ 21 eV/atom. This corresponds to a D_c value of ~ 5.7 x 10^{14}/cm^2. The difference in RT E_c values for the two implanted species is ~3 eV/atom which is slightly higher than was the case for LN results. The average energy of amorphization of SiC at RT is then ~ 22.5 eV/atom.

A summary of the above implantation conditions and results is given in Table I. As noted above, E_c increases with an increase in implantation temperature. This is expected, since the addition of energy to the lattice in the form of heat, increases atom mobility which, in turn, can result in in-situ annealing of implantation-induced damage. Therefore, it would require an increase in dosimetry (D_c) to cause amorphization of the lattice. In turn, an increase in damage energy deposited, or E_c, is required.

The value of E_c at a given temperature does vary slightly for the two implanted species utilized in this research. There are approximations in these analyses that should be noted. Two exist with regard to the theoretical damage energy profile obtained using the Monte Carlo program, TRIM. Firstly, it is assumed that the slowing and scattering of energetic ions occurs in an amorphous target. However, crystalline SiC is used in our



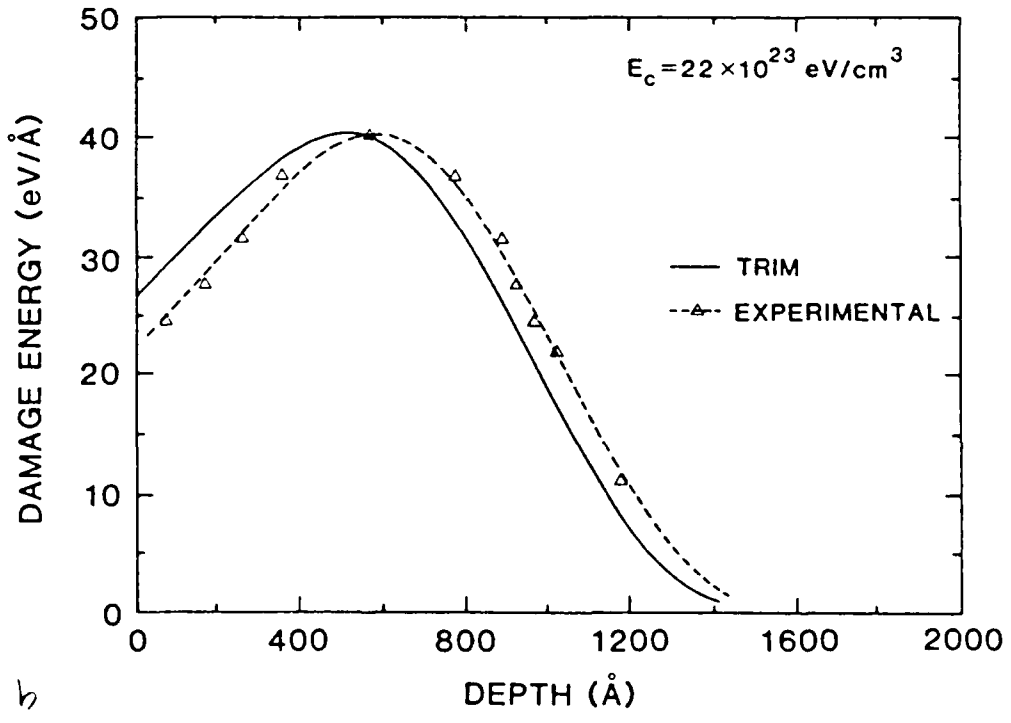


Fig. 8. (a) 2.0 MeV He^+ backscattering spectra for 87 keV RT Si-implanted β-SiC along [100], and (b) the corresponding TRIM and experimental damage energy profiles.

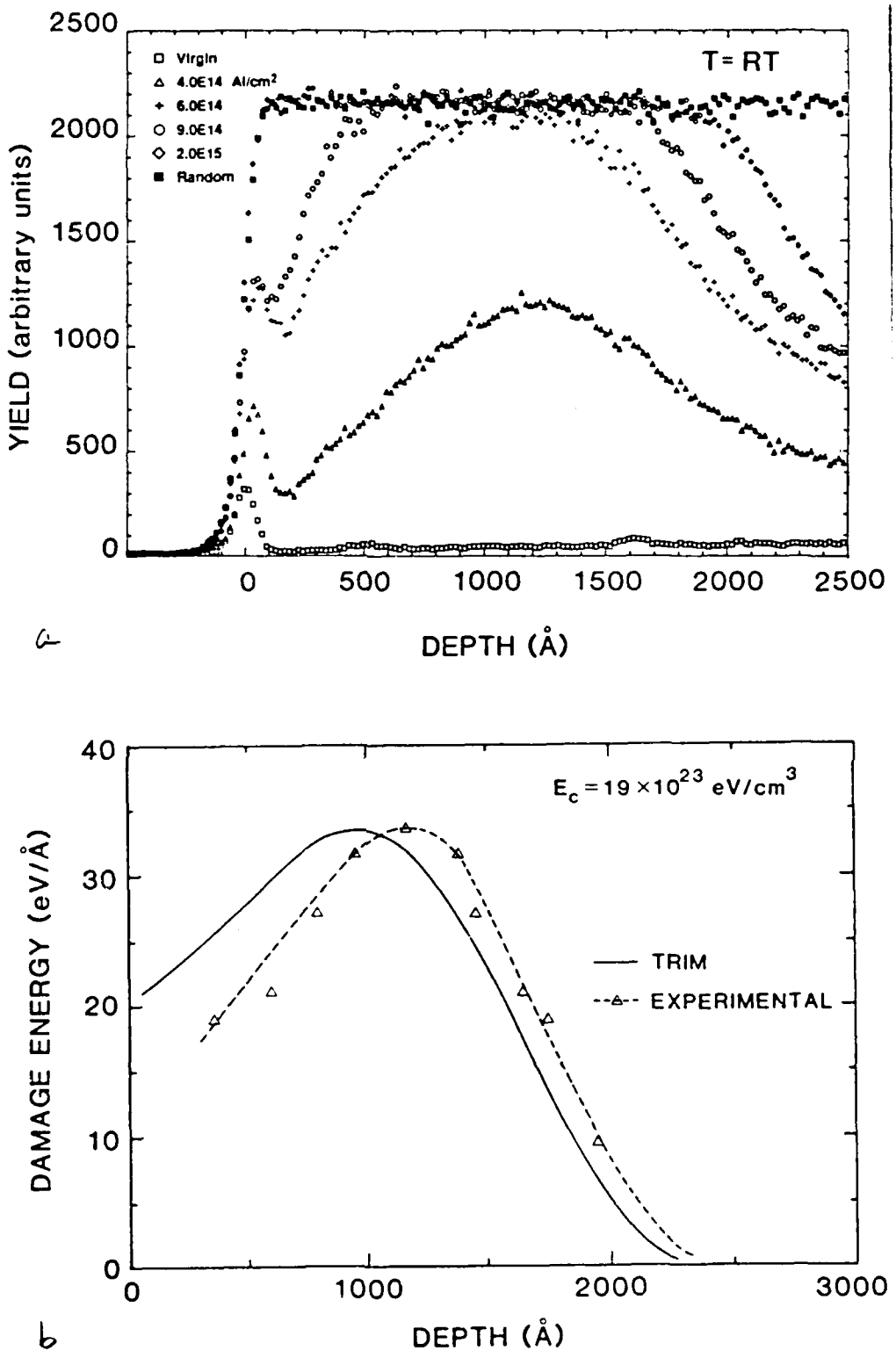


Fig. 9. (a) 2.0 MeV He^+ backscattering spectra for 130 keV RT Al-implanted β-SiC along [100], and (b) the corresponding TRIM and experimental damage energy profiles.

Table I. Implantation Conditions and Results for Determination of E_c

87 keV $^{28}Si^+$			130 keV $^{27}Al^+$		
Temp	Dose x 10^{14} (cm^{-2})	Amorphous Layer Depth (nm)*	Temp	Dose x 10^{14} (cm^{-2})	Amorphous Layer Depth (nm)*
LN	4.0	30 - 79	LN	4.0	75 - 133
	5.0	21 - 85		5.0	65 - 145
	6.0	5 - 95		6.0	45 - 150
	8.0	0 - 103		7.0	27 - 163
	10.0	0 - 110		8.0	17 - 172
				10.0	0 - 178
	$D_c = 3.5 \times 10^{14}\ cm^{-2}$			$D_c = 3.7 \times 10^{14} cm^{-2}$	
	$E_c = 15$ eV/atom			$E_c = 14$ eV/atom	
RT	6.0	36 - 78	RT	6.0	96 - 139
	7.0	26 - 89		7.0	80 - 146
	8.0	17 - 93		9.0	60 - 165
	9.0	8 - 97		10.0	36 - 175
	10.0	0 - 103		20.0	0 - 195
	20.0	0 - 118			
	$D_c = 5.5 \times 10^{14}\ cm^{-2}$			$D_c = 5.7 \times 10^{14} cm^{-2}$	
	$E_c = 24$ eV/atom			$E_c = 21$ eV/atom	

* These values refer to the positions of the beginning and end of the amorphous layer referenced to the surface (depth = 0) of the SiC film.

analyses. To approximate implantation in a random structure, one misaligns the beam from any major crystallographic direction. In our research, a 7° offset was employed. However, channeling of the implanted beam can and, to a small degree, does occur under these conditions [8]. This could result in damage being created at a greater depth than is predicted by TRIM. Indeed this is observed, to some extent, in all the damage energy plots previously discussed. This deviation is less pronounced in the LN-implanted samples, perhaps as a result of a lower E_c. This indicates local amorphization occurs earlier in the amorphization process than that which would occur in a more energetic lattice. A second possible source of deviation in results may be the method in which the program computes damage production from recoils. The recoils are not individually followed in the program but rather the amount of damage they produce is approximated through the use of theoretical calculations (see p. 268 in Ref. 7). The effect of this approximation on our results is not clearly known. However, the authors are presently investigating a recently upgraded Monte Carlo program *(TRIM Cascades)* that does track damage production from recoils as well as from the primary ions

SUMMARY

The techniques of RBS/C and TEM have been used together to investigate the radiation damage along 3 directions resulting from Al ion implantation in SiC at LN temperatures. Enhanced backscattering in the [110] and [111] directions occurred as a result of a 2% lattice expansion in the [100] direction, making invalid the use of RBS/C spectra along these axes as a means of predicting E_c for SiC. An accurate measure of determining the depths at which amorphization occurs was obtained by channeling along [100]. From this, damage production in SiC at LN and RT was studied. These results were coupled with those obtained from TRIM and the critical energy for amorphization of SiC at LN and RT was determined to be ~ 14.5 and ~ 22.5 eV/atom, respectively.

ACKNOWLEDGEMENTS

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VI. STRUCTURAL CHARACTERIZATION OF ION IMPLANTED ß-SiC THIN FILMS

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ABSTRACT

Thin films of ß-SiC (100) grown on Si, have been implanted with Al, P, Si and Si plus C. The temperature dependence of implantation-induced damage was studied between 77K and 1023K using transmission electron microscopy and Rutherford backscattering/channeling. Amorphous layers resulting from implantation of any of the above species recrystallized via solid-phase-epitaxy during post-implantation annealing between 1973K and 2073K. As such, this latter process necessitated the prior removal of the Si substrate. However, the resultant layers were very defective. Increasing the sample temperature to 1023K during implantation allowed in situ dynamic annealing of the samples and therefore, greatly reduced the residual damage to the lattice. No additional annealing was required for structural recovery.

I. Introduction

Cubic (zincblende structure) beta-SiC is the principal and perennial candidate material for electronic devices for operating under one or more of the conditions of high temperature, high power or high speed. The resurgence in interest in this material has been driven by (1) the increased need for devices operable under the aforenoted conditions, (2) the fact that the recent advances in Si-based thin film deposition and device fabrication technologies can, in most cases, be directly translated to SiC, and (3) the drive to achieve very large numbers of integrated devices per unit area. As the planar density of devices

increases, the thermal load and management become major problems. However, the high thermal conductivity of SiC (5 W/cm-deg – approximately that of W) will allow the necessary dissipation of heat and thus the desired large scale device integration without degradation in device performance.

An unstated but critical factor underlying some of the above comments is that the operation of most electronic devices require that the material be amenable to doping with both n (donor) – and p (acceptor) – type dopants. This has been accomplished in SiC but not in GaN or C (diamond) – the two rival materials for devices for employment under severe conditions.

Two common methods of doping SiC have been in situ incorporation from the gas phase during growth and from diffusion sources at high temperatures. An alternative method of controllably introducing impurities, and one more suitable for device fabrication in SiC, is ion implantation.

In the process of ion implantation, nuclear scattering events occur inside the host material during the deceleration of an implanted atom and result in regions containing lattice damage. As the dose (ions/cm^2) of the implanted specie is increased, the near-surface region of the implanted material becomes progressively damaged; atomic disorder and eventual amorphization of the structure occurs. Early work by Hart et al.[1] utilized Rutherford Backscattering/channeling (RBS/C) techniques in order to study both disorder production in monocrystalline 6H α-SiC by ion implantation of Sb and N at room temperature and the subsequent structural recovery of the lattice during thermal annealing. They showed that the amorphous regions reordered considerably upon annealing at 923K. However, the extent of the residual line and planar defects present after annealing was not determined.

More recently, cross-sectional transmission electron microscopy (TEM) has been used to show that regrowth of amorphous layers produced via ion implantation invariably

occurs by solid-phase epitaxy (SPE) from existing crystalline surfaces[2]. However, the results of this research have also shown that the quality of these SPE regrown layers in compound semiconductors is generally very poor. The two major problems are that nonstoichiometry results during implantation and that dissociation of the constituent elements of the compound semiconductor usually occurs at different temperatures during thermal annealing. Finally, the need for regrowth may be ameliorated or even eliminated by implantation at an elevated temperature sufficient to cause dynamic annealing of the damage.

In the present research, ion implanted layers were produced in monocrystalline ß-SiC thin films at liquid nitrogen (LN), room (RT) and high temperatures ($T \geq 673K$) and characterized using cross-sectional TEM and/or RBS/C. These results as well as those determined from samples subjected to post implantation annealing will be presented.

II. Experimental Procedures

Thin films of ß-SiC were epitaxially grown in-house on silicon (100) wafers via chemical vapor deposition.[3] Prior to implantation each sample was mechanically polished, oxidized, and etched in HF in order to obtain a clean, undamaged and smooth surface. After mounting in high vacuum, samples were implanted at LN, RT or high temperature ($T \geq 673K$) with either Al, P, Si or Si and C. The first two species were implanted in order to dope ß-SiC p-type and n-type, respectively; the latter two were used for preamorphization prior to subsequent dopant introduction at concentrations below which amorphization occurs. All implants were made at an incident angle 7° off normal to avoid channeling effects. A summary of implant species and conditions is given in Table I.

Following implantation under LN or RT conditions, samples to be characterized in TEM were sectioned in half. One section was used to observe the as-implanted damage;

Table I. Summary of Ion Implantation Conditions

Figure No.	Ion Species	Energies(keV)	Doses(cm^{-2})	*Peak Atomic Conc.(cm^{-3})	Implant Temp(K)
1	$^{27}Al^+$	130	$1x10^{15}$	$1x10^{20}$	77
2	$^{31}P^+$	110,220	$6,10x10^{14}$	$1x10^{20}$	77
3(B)	$^{28}Si^+$	120,160,320	$2.3,3.2,5.1x10^{14}$	$3x10^{19}$	77
(C)	$(3(B)+)^{12}C^+$	50,67,141	$2.7,3.2,4.8x10^{14}$	$3x10^{19}$	77
4	$^{27}Al^+$	110,190	$6,9x10^{14}$	$1x10^{20}$	298
5	$^{31}P^+$	110	$7.7x10^{13}$	$1x10^{19}$	298
6(A)	$^{31}P^+$	110	$1x10^{15}$	$1x10^{20}$	298
(B)	$^{31}P^+$	110	$1x10^{15}$	$1x10^{20}$	77
8(A)	$^{27}Al^+$	130	$4x10^{14}$	$4x10^{19}$	1023
(B)	$^{27}Al^+$	130	$4x10^{14}$	$4x10^{19}$	77

*Peak concentration values determined by LSS calculation

the other was used in annealing experiments. (Samples implanted at high temperature were not sectioned or annealed.) Before annealing, films were separated from the Si substrate on which they were grown by etching in an (1:1) $HF:HNO_3$ solution until the Si was dissolved. The thickness of each film was approximately 15 μm. Upon loading a sample, the annealing chamber was evacuated to a pressure of 10^{-5} Torr and backfilled with Ar to a pressure ~1 atmosphere. Argon was used in order to help reduce the rate of Si loss during the heating of SiC. Sample halves were annealed at 1973K - 2073K for a period of 300 s. Cross-sectional TEM samples of these implanted materials were prepared for observation, as discussed in Ref. 4.

Backscattering spectra as well as cross-section TEM results were also obtained on ß-SiC implanted with Al at RT, 623K, 823K and 1023K to study the effect of in situ annealing during implantation. The RBS/C analyses were performed using 2.0 MeV $^4He^+$ ions incident along the [110] axial direction.

III. Results and Discussion

(1) LN Implantation of Al and P

Figure 1 shows cross-sectional TEM micrographs of a sample implanted under LN conditions with Al to a peak atomic concentration of 10^{20} Al/cm^3. This concentration is

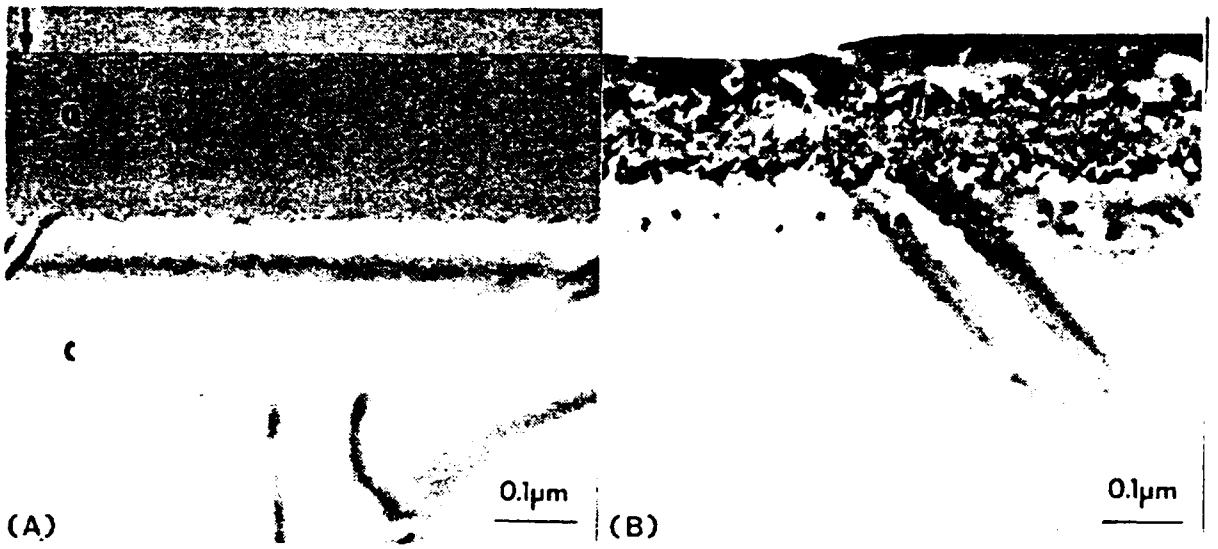

Fig. 1. Cross-sectional TEM micrographs showing the near-surface region of a sample which has been implanted at LN temperature with Al to a peak concentration of 10^{20} Al/cm^3. (A) As-implanted, (B) annealed at 1973K for 300 s.

typical for forming a p-type layer in our material. During implantation, the surface became amorphous to a depth of ~0.20 μm, as shown in Fig. 1(A). Thermal annealing of this sample at 1973K caused the layer to recrystallize. As shown in Fig. 1(B), a line of defects, commonly referred to as straggling ion damage, resulted near the original lower amorphous-crystalline (a-c) interface. Additionally, a broad band of polycrystalline SiC formed within the central region of the original amorphous layer. This band is bounded by single crystal material with the same crystallographic orientation as the bulk crystal. Three growth mechanisms by which the observed microstructures could have resulted are described below.

There are two possibilities if one assumes the layer to be amorphous to the very surface following implantation. Firstly, the high free energy associated with a surface could result in heterogeneous nucleation and growth from that surface during annealing. Likewise, SPE from the lower a-c interface would occur. The convergence of these two growth fronts could result in a polycrystalline layer centered about the implant peak, as was experimentally observed. Secondly, SPE could occur from the lower a-c interface only. In this case, single crystal growth could initially occur, become textured polycrystalline in the region of the implant peak where the highest concentration of Al exists, and return to single crystal as the Al concentration decreases toward the surface.

The third possible growth mechanism assumes that a thin crystalline cap, not visible at the magnification used to obtain Fig. 1(A), remains following this implant. Under these conditions, SPE could occur from both the lower and upper a-c interfaces during annealing which would again lead to convergence of the moving growth fronts within the region of maximum Al concentration.

Figure 2 illustrates the regrowth properties a P double implant with a peak concentration of 10^{20} P/cm^3. An ~0.5 μm amorphous layer was created similar in appearance to that shown in Fig. 1(A). The annealing temperature was 1973K. A polycrystalline layer also resulted, in this case, after ~0.1 μm of single crystal regowth from the lower a-c interface. Straggling ion damage was also observed in the a-c region. The solubility limit of this element in our films during growth at 1660K has recently been determined to be ~10^{18} P/cm^3.[5] Although the annealing temperature of 1973K exceeds the growth temperature, it is believed that the P became supersaturated at the growth front and subsequently formed precipitates which caused the onset of polycrystallinity.

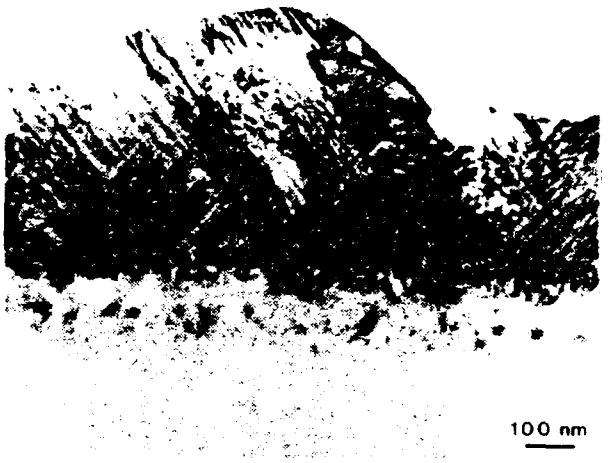

Fig.2. Cross-sectional TEM micrograph of a sample which has been implanted at LN temperature with P to a peak concentration of 10^{20} P/cm^3 and subsequently annealed at 1973K for 300 s. The near-surface region appears rough as a result of polycrystalline regrowth.

(2) LN Implantation of Si and Si plus C

As seen in Figs. 1(B) and 2, straggling ion damage usually occurred at the original a-c interface following annealing. This damage may cause high leakage currents in diodes, for example, since the damage is near the electrical junction. An increasingly popular method of circumventing this problem is to conduct a high-energy implant of an electrically neutral species prior to implanting the dopant at a lower energy in order to create a deep amorphous layer. As a result, the defects that form after annealing will be relatively far away from the electrical junction. This method also allows complete activation of the dopant for low dose implants and produces sharper dopant profiles, since it prevents channeling of the dopant ion. In an attempt to achieve these effects in ß-SiC, films from our research were implanted with self-ions.

The cross-sectional TEM micrographs in Fig. 3 directly compare the structural regrowth properties of implanted and amorphized layers created using Si and Si plus C. Figure 3(A) shows the amorphous layer which was formed by triple implantation of Si to a

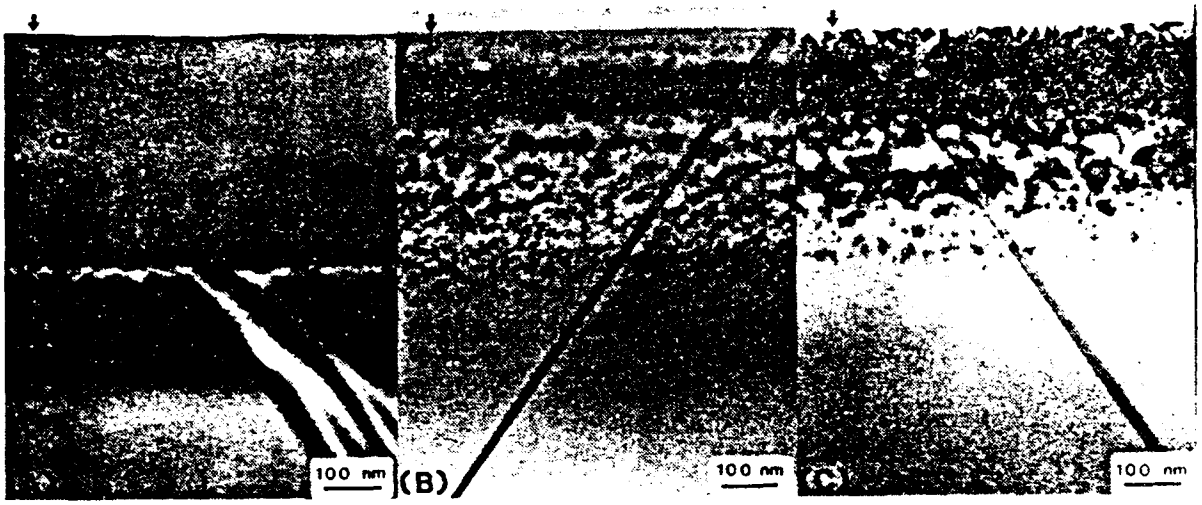

Fig. 3. Cross-sectional TEM micrographs comparing the regrowth properties of samples implanted under LN conditions with equal atom concentrations ($3x10^{19}$ cm^{-3}) of Si (B, center) and Si + C (C, right). The as-implanted amorphous layer is also shown in (A). Samples were annealed at 1973K for 300 s.

peak concentration of 3 x 10^{19} Si/cm^3. The a-c interface is located ~0.40 μm below the sample surface. After anneling at 1973K, the layer regrew epitaxially without the severe faulting noted above. However, a high concentration of precipitates and/or loops formed throughout the regrown bulk. In an attempt to eliminate these defects, a triple C implant was superimposed on the triple Si implant thus simulating implantation of SiC into SiC. The projected range peaks were matched (1:1) Si to C using LSS theory[6] in order to obtain the correct stoichiometry. Figure 3(C) shows a cross-sectional TEM micrograph of the regrown layer previously implanted and amorphized with SiC at a peak concentration of 3 x 10^{19} for both species. The annealing conditions were the same as described for the sample shown in Fig. 3(B). Quite clearly, implanting Si plus C did not structurally improve the quality of the region layer. In fact, microfaulting and microtwinning occurred upon regrowth from ~0.14 μm to the sample surface.

(3) RT Implantation of Al and P

Figure 4 shows cross-sectional TEM micrographs of ß-SiC double implanted with Al at RT to a peak concentration of 10^{20} Al/cm^3. A buried amorphous layer having a crystalline cap of ~0.01 μm resulted after implantation (Fig. 4(A)). This upper. and the

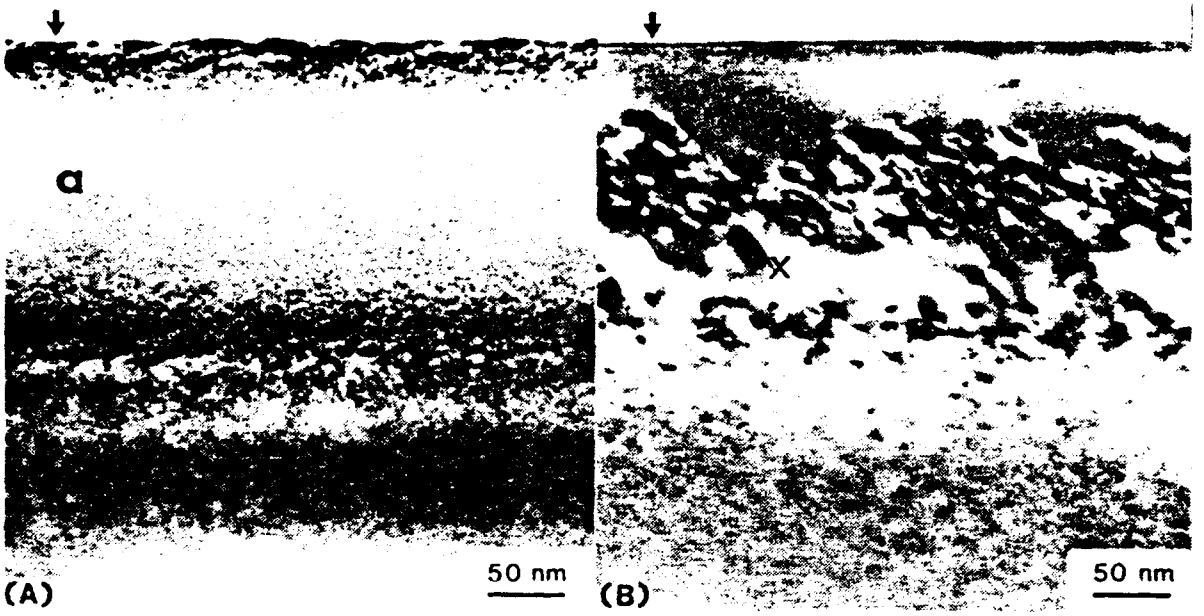

Fig. 4. Cross-sectional TEM micrographs showing the near-surface region of a sample which has been implanted at RT with Al to a peak concentration of 10^{20} Al/cm^3. (A) As-implanted, (B) annealed at 2073K for 300 s. X denotes microfaulted regions.

lower a-c interface located at a depth of ~0.17 μm, were very diffuse as a result of implanting at RT. After annealing at 2073K, the amorphous layer regrew by SPE. However, a high concentration of defects was observed (Fig. 4(B)). Precipitates and/or dislocation loops formed where the lower a-c interface was initially located. A broad band of defects (0.05 - 0.11 μm) resulted where the two a-c interfaces converged during SPE regrowth. Unlike the previous Al implant, however, this region was single crystal with precipitates and some microfaulting (see areas labeled X in Fig. 4(B)). Additionally, approximately the first 0.05 μm below the surface proved to be virtually free of the

planar and line defects.

In order to prevent amorphous layer formation during P implantation, and subsequently, polycrystalline regrowth, (as was described in Section (1)), a lower dose RT implant was implemented. The peak atomic concentration was 10^{19} P/cm^3. Evidence of implant damage appeared as a band of dark contrast parallel to the surface in the as-implanted material (Fig. 5(A)). This dark band was not amorphous since stacking faults were visible in this area. After annealing at 2073K, the band of dark contrast was replaced by defect clusters (Fig. 5(B)). No second-phase diffraction spots were observed in selected area diffraction patterns generated from the P-implanted region.

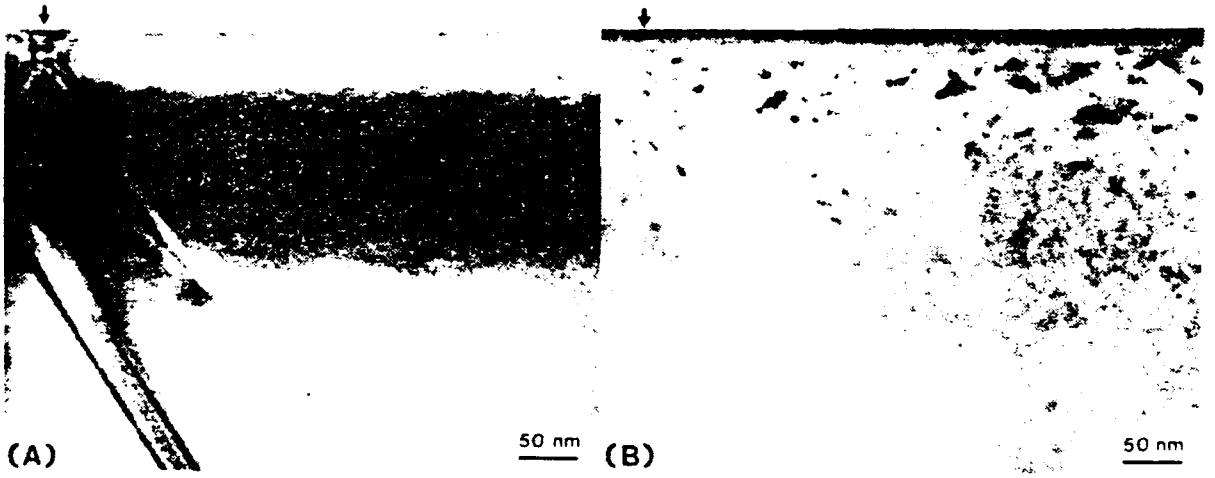

Fig. 5. Cross-sectional TEM micrographs showing the near-surface region of a sample implanted at RT with P to a peak concentration of 10^{19} P/cm^3. (A) As-implanted, (B) annealed at 2073K for 300 s.

The effect of the implant temperature on the extent of amorphization is illustrated in Fig. 6. Both micrographs are of films that were implanted with P to a peak concentration of 10^{20} P/cm^3, but the sample in Fig. 6(A) was implanted at RT while the sample in Fig. 6(B) was maintained under LN conditions. The RT sample had a ~0.01 μm crystalline

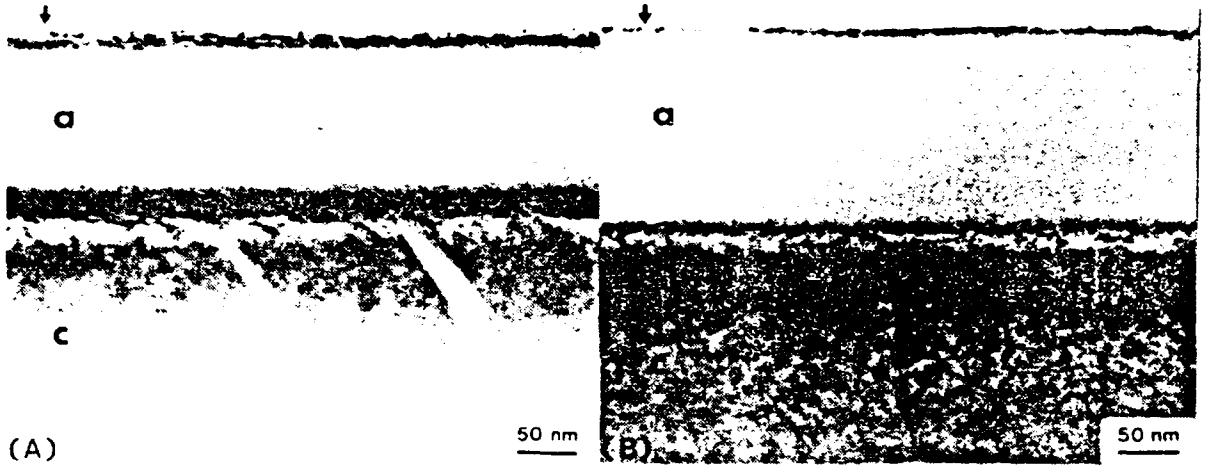

Fig. 6. Cross-sectional TEM micrographs comparing the near-surface damages created by implantation of P to a peak concentration of 10^{20} P/cm^3 under (A) RT and (B) LN conditions.

surface, an amorphous depth of ~0.13 μm, and visible damage to ~0.23 μm. The LN implant created a thinner crystalline cap (~0.005 μm), an amorphous depth of ~0.17 μm, and visible damage to ~0.35 μm. The same effect of similar magnitude has been observe in Si wafers implanted at RT and LN.[6] This similarity was unexpected, as the melting temperature of SiC is > 3073K, while that of Si is 1679K. These results led the authors to the notion that heating ß-SiC above RT during implantation may result in in situ annealing of lattice damage. The results of the high temperature (HT) implantation experiments are given below.

(4) HT Implantation of Al

The effect of sample heating during implantation on damage production was investigated using Al implants produced at RT, 623K, 823K and 1023K. Figure 7 compares RBS/C spectra for samples implanted at these four temperatures to a peak concentration of 7 x 10^{19} Al/cm^3. As shown in this figure, a buried amorphous layer was created within the near-surface region after RT implantation. Heating similar samples to

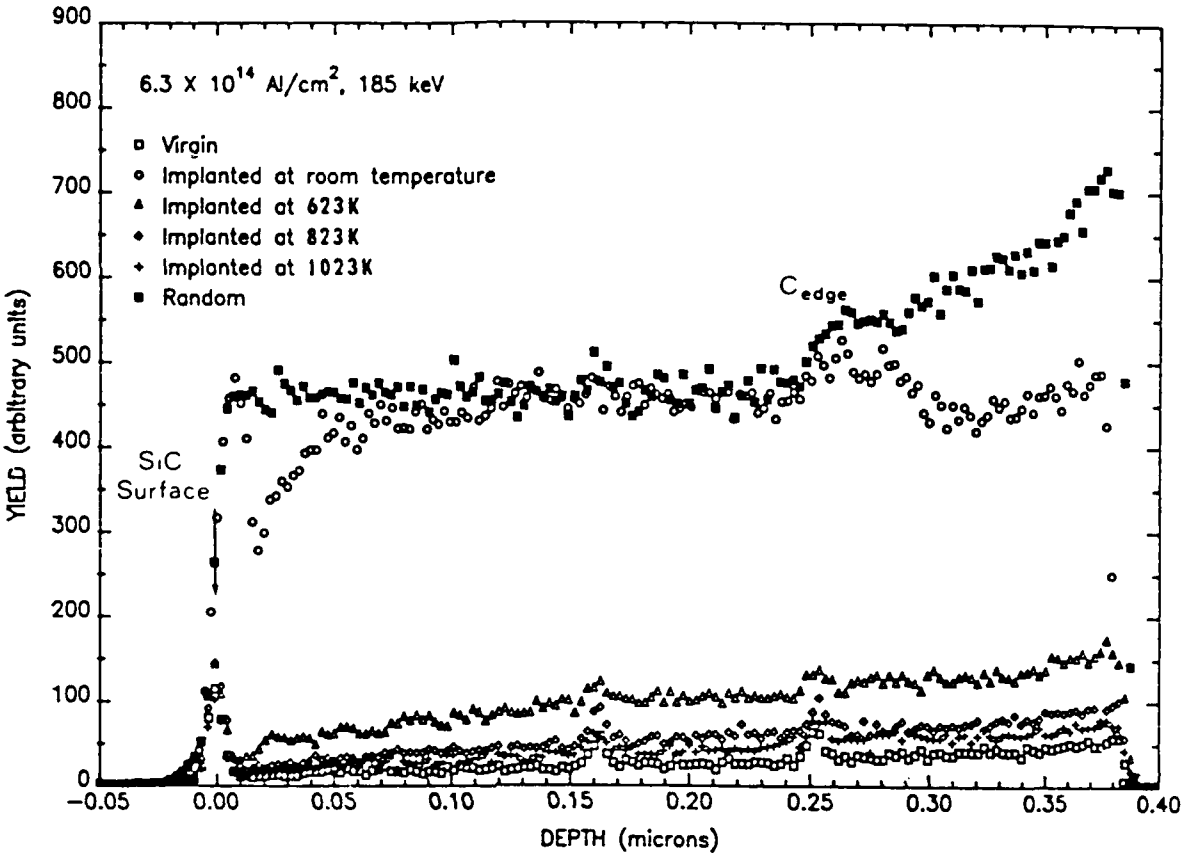

Fig. 7. 2.0 MeV He RBS/C spectra for Al-implanted ß-SiC showing the decrease in lattice damage along [110] with an increase in implant temperature.

623K and higher temperatures during implantation progressively reduced the induced damage. The spectra from the 1023K implants nearly coincided with that of the virgin aligned. This latter spectrum is taken from an unimplanted region adjacent to the implanted area. Therefore, the crystallinity of the lattice was virtually recovered during HT implantation, within the sensitivity of RBS/C. However, this technique is not as sensitive to line and planar defects as is TEM. For that reason, two ß-SiC samples, implanted under like conditions except temperature, were analyzed in TEM.

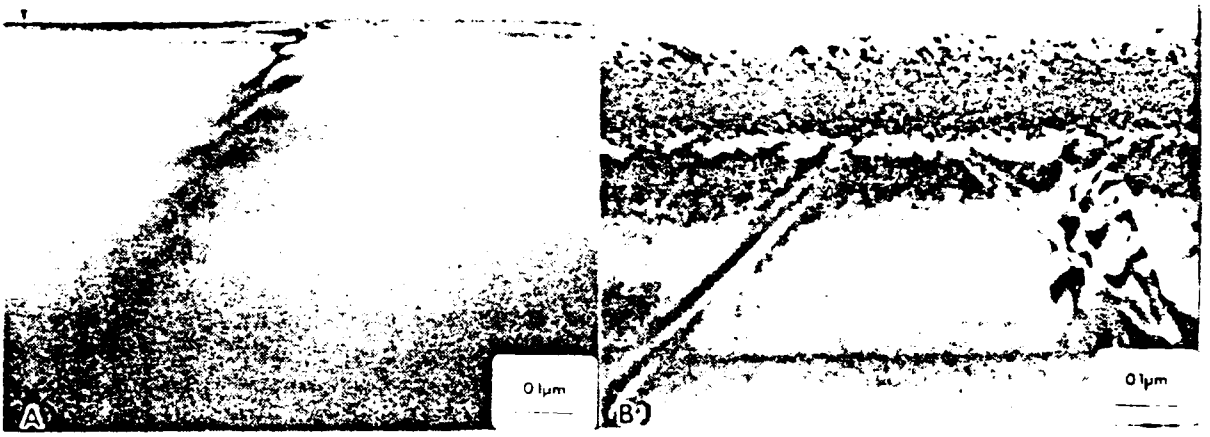

Fig. 8. Cross-sectional TEM micrographs comparing the near-surface damage created by implantation of Al to a peak concentration of $4x10^{19}$ Al/cm^3 at (A) 1023K and (B) LN temperature.

Figures 8(A) and 8(B) illustrate the damage produced during implantation of Al in ß-SiC at 1023K and 77K, respectively. As shown in Fig. 8(A), implantation at 1023K resulted in neither visible lattice damage nor precipitates. The implant under LN conditions resulted in the creation of a buried amorphous layer. Upon annealing the latter sample to 1973K, residual defects similar to those obtained in Fig. 4(B) were observed. Annealing at this high temperature required Si removal; whereas, annealing to 1023K during implantation did not. This is yet another advantage to high temperature implantation in this material.

III. Summary and Conclusions

Ion implantation of Al, P, Si and Si plus C into single crystal ß-SiC thin films was performed. The temperature dependence of implantation-induced damage was studied between 77K and 1023K. It was determined that amorphous layers produced in ß-SiC regrew via SPE in the temperature range of 1973K - 2073K. In all cases, however, the

quality of regrown regions were very poor; various combinations of precipitates, dislocation loops, microfaults and polycrystalline regions often resulted. It was shown that heating the sample as low as RT during implantation, reduced the width of the amorphous layer that resulted from LN implantation. Finally, it was shown that implantation at higher temperature (623K - 1023K) resulted in structural recovery of a layer during ion bombardment. This allows one to introduce electrically active dopants into ß-SiC controllably without damaging the crystal lattice and just as importantly, doing so without having to remove the silicon substrates on which they are grown.

Acknowledgement: The authors gratefully acknowledge the support of this program by the Office of Naval Research under contract N00014-82-K-0182 P005 and to the ONR Fellowship program for support of one of the authors (Edmond). Work at Oak Ridge National Laboratory was supported by the Division of Materials Sciences, U.S. Department of Energy under contract DE-AC05-840R21400 with Martin Marietta Energy Systems, Inc. Appreciation is also expressed to C.H. Carter, Jr. for assistance in the preparation and interpretation of the TEM micrographs.

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VII. ELECTRICAL PROPERTIES OF ION IMPLANTED P-N JUNCTION DIODES IN ß-SiC

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ABSTRACT

Mesa structure junction diodes prepared via high temperature ion implantation of Al^+ (100 keV - $4.8x10^{14}$ Al/cm^2) in n-type or N^+ (90, 180 keV - 0.9, $1.3x10^{14}$ N/cm^2) in p-type ß-SiC thin films were electrically characterized as a function of temperature using current-voltage and capacitance-voltage measurements. In either case, rectification was observed to the highest measurement temperature of 673K. Closer examination of the device current-voltage characteristics yielded diode ideality factors greater than two. Additionally, the log dependence of these two parameters indicated space-charge-limited current in the presence of traps as the dominant conduction mechanism. From the temperature dependence of log-log plots, trap energies and densities were determined. Two trapping levels were observed, (1) 0.22 eV with a density of $2x10^{18}$ cm^{-3} and (2) 0.55 eV with a density of $2x10^{16}$ cm^{-3}. The former is believed to be ionized Al centers (in the case of Al-implanted sample) and the latter a compensating acceptor level, both of which lie within the bottom third of the band gap. Reverse currents at low biases were characteristic of generation in the depletion region. At intermediate biases an ohmic dependence was observed whereas at high biases the current appeared to be space-charge-limited. Capacitance-voltage measurements indicated both types of diodes were abrupt junctions.

INTRODUCTION

Cubic (ß) SiC is a wide band gap (E_g = 2.2 eV) semiconductor that possesses physical and electrical properties which make it a principal candidate material for use in high temperature, high power and high speed switching device operations. Recently, several papers have been published regarding the development of devices in this material [1-5]. In particular, Suzuki et al. [2], electrically characterized p-n junction diodes produced by in situ doping during chemical vapor deposition of ß-SiC on Si (100). However, ion implanted junctions in this material have not been reported. Ion implanted junctions in α-SiC were fabricated and characterized by Marsh and Dunlap [6] in 1970. In their research, junctions were formed by room temperature implantation of N (n-type dopant) into p-type material. Implantation of an acceptor specie into an n-type substrate was unsuccessful. By contrast, Kalinina et al. [7,8] were successful in producing p-n junctions in α-SiC using a relatively high range of room temperature implant doses ($3x10^{15}$ - $3x10^{17}$ cm^{-2}) of Al (p-type dopant) and high annealing temperatures (1773K - 2223K).

Production of quality p- and n-type conducting layers formed by high temperature implantation (823K) followed by a relatively low temperature (1473K) anneal have been recently developed in ß-SiC [9]. In the present research, high temperature implantation of Al and N into n- and p-type ß-SiC (100) thin films, respectively, has been performed in order to produce junction diodes. Current-voltage (I-V) and capacitance-voltage (C-V) measurements on these diodes have also been obtained, as illustrated below. Based on these results, a discussion and conclusions regarding the possible current conduction mechanisms that dominate the diode I-V characteristics and estimates of trap energies and densities in our material will be presented.

EXPERIMENTAL

Thin films (10-20 μm) of monocrystalline ß-SiC (100) were epitaxially grown on Si (100) via chemical vapor deposition [10]. Each sample was then mechanically polished, oxidized and etched in HF to obtain a clean, undamaged and smooth surface prior to implantation. After mounting in high vacuum, samples were heated to 823K and implanted with N and Al in p-type ($p \equiv 1x10^{17}$ cm^{-3}) and n-type ($n \equiv 10^{16}$ cm^{-3}) ß-SiC, respectively, to form junctions. The doses and energies of the N dual implant were 0.9, $1.3x10^{14}$ cm^{-2} and 90, 180 keV, respectively; that of the Al implant was $4.8x10^{14}$ cm^{-2} and 100 keV. The implants were made at an incident angle of 7° off normal to avoid channeling effects. Following implantation, each sample was annealed at 1473K for 1800 s in dry O_2 followed by the same temperature and time in Ar and then etched in HF. This procedure provides a means of structurally healing the implanted region and activating the dopant while removing ~ 20 nm of a Si-rich near-surface region resulting from implantation.

Mesa structure diodes (n-p and p-n) were fabricated on both N- and Al-implanted ß-SiC, respectively. The mesa structures were formed with an area of $3.14x10^{-4}$ cm^2 by reactive ion etching with NF_3 gas [11] using Al as a mask for etching. Ohmic contacts for p- and n-type material were Al and $TaSi_2$, respectively [12].

Current-voltage measurements between 300K and 673K and room temperature C-V measurements were performed to electrically characterize the fabricated diodes. A Hewlett-Packard 4145A Semiconductor Parameter Analyzer and Materials Development Corp. RM1600 C-V System, respectively, with a Rucker and Kolls 260 probe station were used for these measurements. The hot-stage assembly, constructed in-house, consisted of two cartridge heaters in a BN block on porous Al_2O_3 board. All measurements were made in air.

RESULTS

a) N-implanted Junctions

Typical linear I-V plots of the N-implanted mesa diodes described above are shown in Fig. 1. Measurements were made between 300K and 673K. Clearly, the diode is

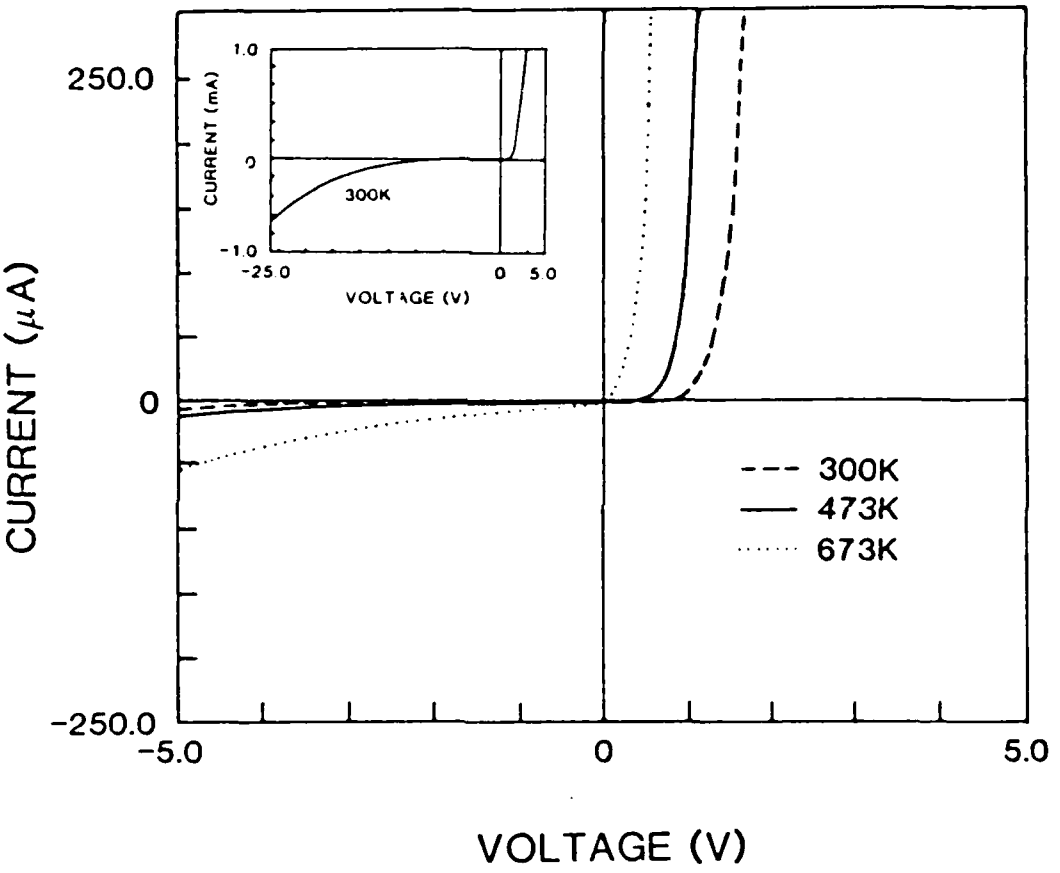


Fig. 1. Linear current-voltage characteristics for a N-implanted junction diode in ß-SiC a function of temperature.

rectifying with relatively low leakage current (I_L). At a reverse bias of 5 V, the room temperature I_L was ~5 μA. The room temperature reverse current increased moderately with increasing bias, as shown in the inset in Fig. 1. At the highest measurement temperature, I_L increased to ~50 μA at -5 V. In the forward bias, a turn-on voltage of

~ 1 V was observed at 300K which reduced to essentially 0 V at 673K.

Figures 2a and 2b illustrate the semilogarithmic plots of current density (J) versus V, for the above diode in forward and reverse bias, respectively, up to 2.5 V and 673K. As shown in Fig. 2a, the J-V characteristics at low levels of injection (V<1 V) exhibited an exponential dependence. Assuming that this exponential dependence can be given by,

$$J \propto \exp\left(\frac{qV}{nkT}\right) \qquad (1)$$

where q is the electron charge, k is Boltzman's constant and T is temperature, then the diode ideality factor, n, decreased from ~3.8 at 300K to ~2.0 at 673K. These values of n do not fall within the range that result when diffusion current (n=1) or recombination current (n=2) dominate the forward bias current conduction. Following the exponential regime a change of slope occurred which may be indicitive of high-level injection. This effect is pronounced in the 300K and 373K plots. At the highest voltages, the series resistance effect appears to dominate.

Figure 2b illustrates the corresponding reverse bias characteristics of the above diode. From the 300K curve it becomes obvious that current generation other than pure drift dominates the reverse characteristics. As expected, this current increased with increasing temperature.

In order to more clearly understand the electrical characteristics of these p-n junctions in ß-SiC, log J-log V measurements were plotted. Figures 3a and 3b illustrate the forward and reverse bias properties, respectively, to 10 V at 300K and 473K. For the 300K plot in Fig. 3a, two approximately linear regimes existed separated by a sharp rise in current. At low voltages ($V \leq 0.1$ V) an ohmic relationship ($J \propto V$) was observed (noise prevented measurement at ≤4 mV). At V>1 V the current rose sharply to another essentially linear region where $J \propto V^2$. Measurement at 473K yielded similar results. However, at low voltage there now appeared to be two linear regions with $J \propto V$ followed

by $J \propto V^{1.7}$. This was again followed by an increase in current to a third linear region where $J \propto V^{1.7}$. As will be discussed later, these phenomena are characteristic of current conduction in an insulator with shallow and/or deep traps and thermally generated carriers. If one draws parallel lines through the upper and lower linear regions of the current where $J \propto V^{1.7}$ and takes the ratio J_{low}/J_{high} (at any given voltage) as a function of temperature, one can obtain a value of trap energy and density [13-15]. This ratio, referred to as θ, is the probability of trap occupation. The relationship between θ, trap density (N_t) and trap energy (E_t) is:

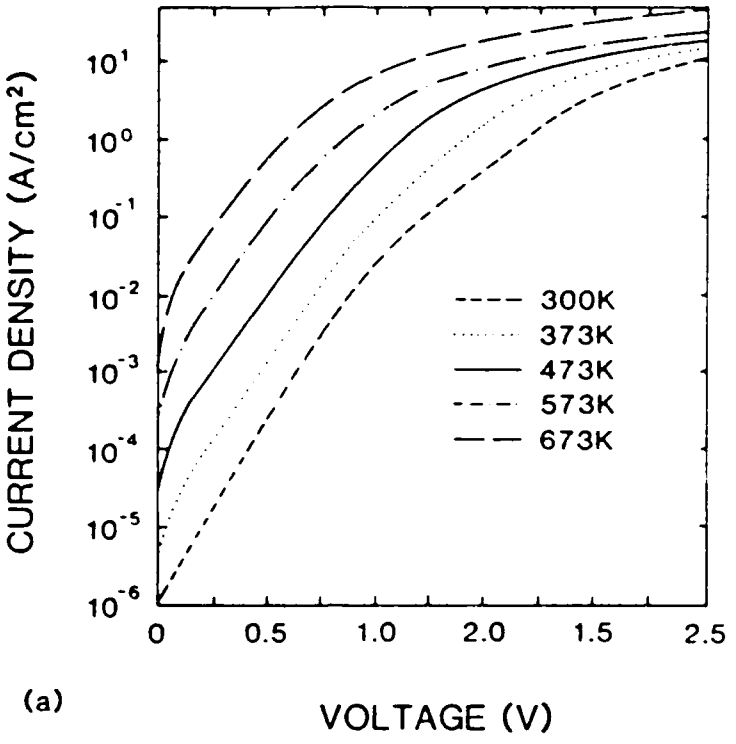
$$\theta = \frac{N_{v,c}}{N_t} \exp\left(-\frac{E_t}{kT}\right) \qquad (2)$$

where $N_{V,C}$ is the effective density of states in the valence or conduction band in the case of hole or electron traps, respectively.

Figure 4 shows the plot of log θ vs. $1/T$ for N-*implanted* ß-SiC diodes. As shown, a straight line relationship was obtained for measurement between 473K and 673K, where shallow trapping was observed to dominate the forward current conduction. From the slope and y-intercept of this line, E_t was calculated from Eq. 2 to be 0.55 eV and $N_t = 2 \times 10^{16}$ cm^{-3}, respectively; the latter value was obtained assuming this energy state as an acceptor trap level.

Figure 3b shows the reverse bias log J - log V characteristic of the above diode. With regard to the curve measured at 300K, the relationship between current and voltage at low reverse bias ($V < -0.1$ V) is $J \propto V^{1/2}$, indicative of an abrupt junction. This increased to $J \propto V^2$ and finally $J \propto V^6$. At 473K, the curve exhibits two regions: $J \propto V$ below 1 V and $J \propto V^6$ again at high voltage.

In addition to reverse I-V measurements, capacitance-voltage (C-V) measurements at room temperature were performed on the above diode. Figure 5 shows a plot of $1/C^2$



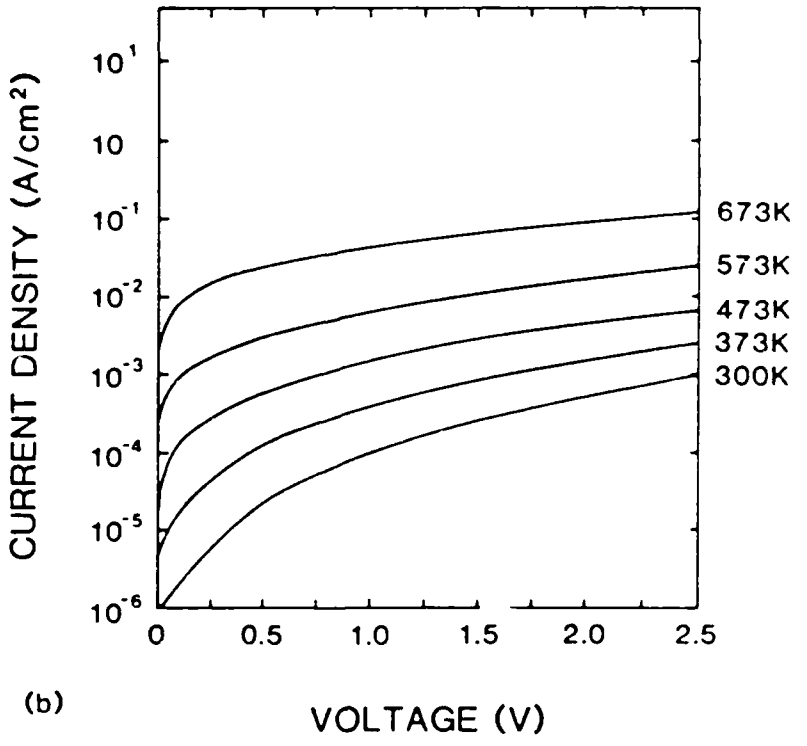


Fig. 2 Temperature dependence of log current density vs. voltage for diode shown in Fig. 1 under (a) forward and (b) reverse bias conditions.

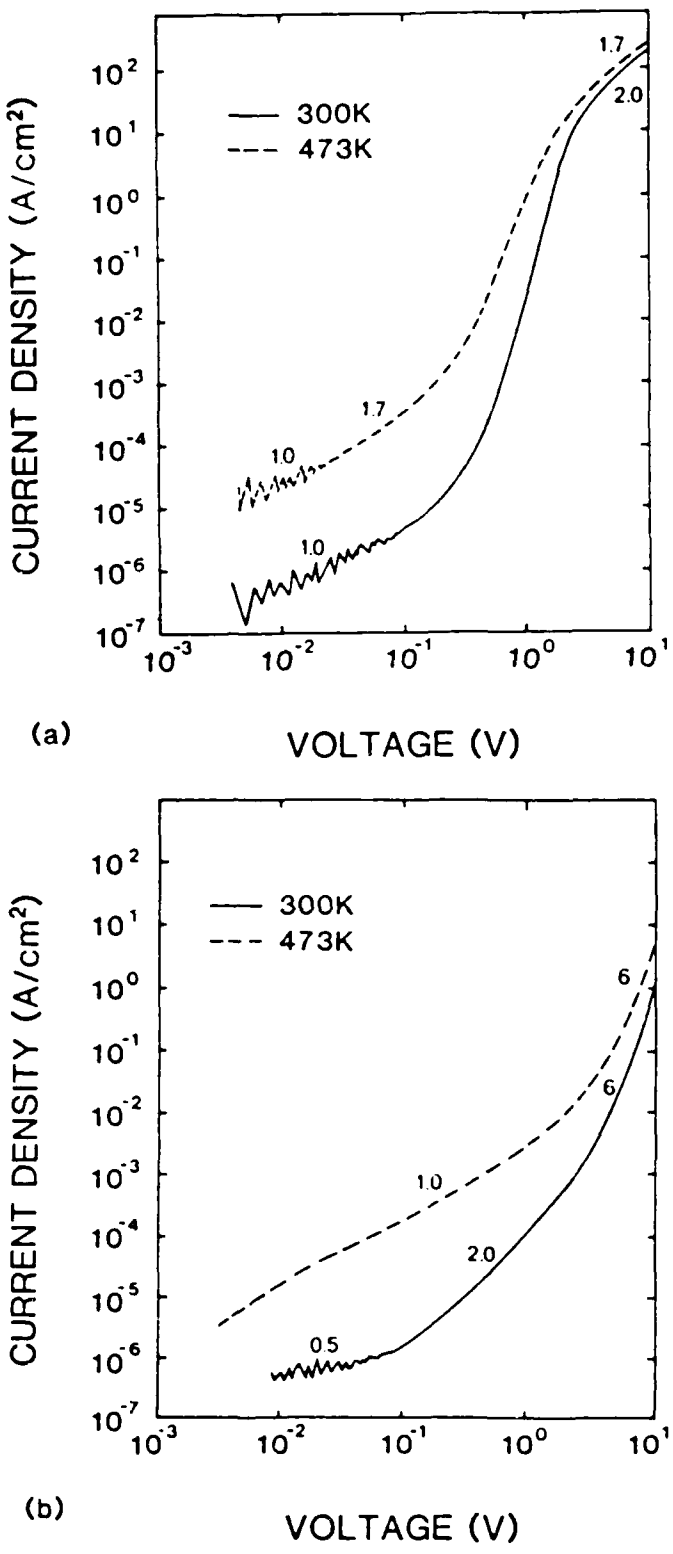


Fig. 3. Temperature dependence of log current density vs. log voltage for diode shown in Fig. 1 under (a) forward and (b) reverse bias conditions. Numbers on linear regions of curves denote the slope, m, where $J \propto V^m$.

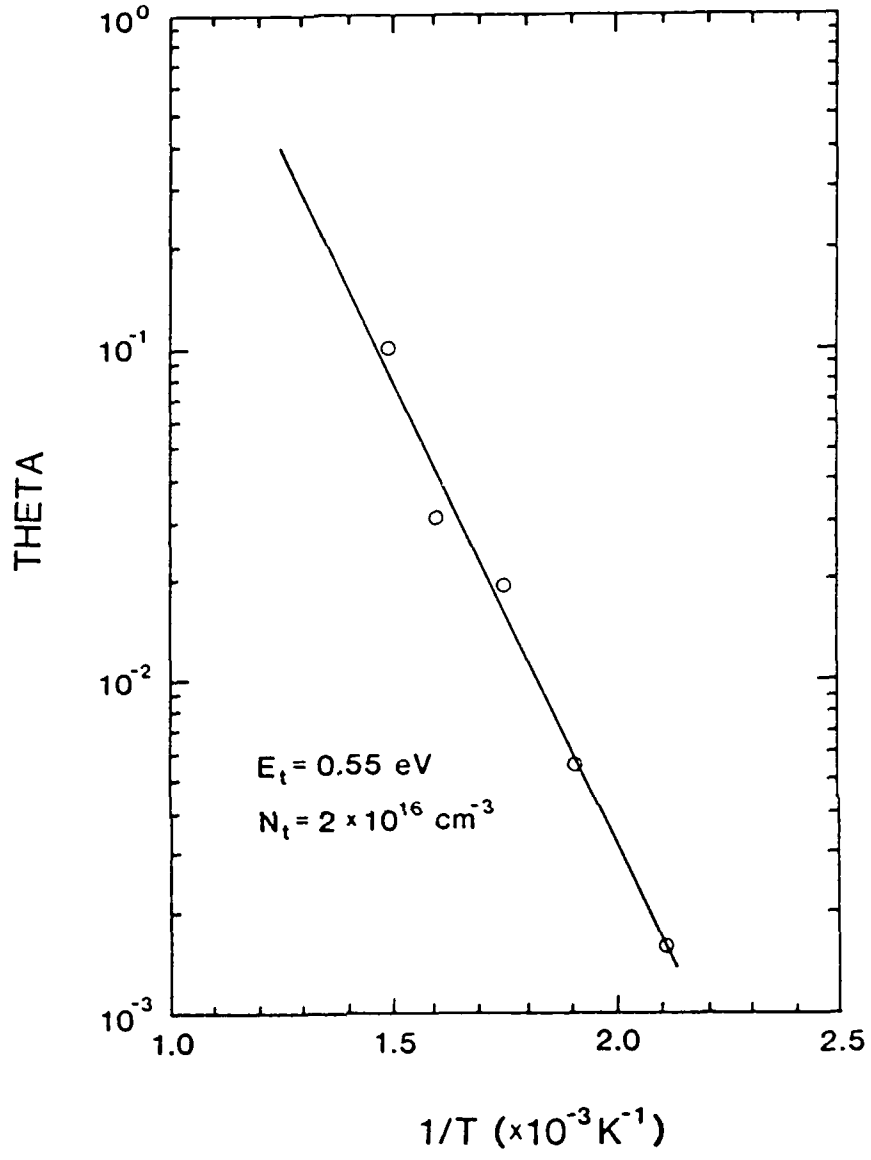


Fig. 4. Plot of log θ vs 1/T to determine trap energy and density in diode shown in Fig.1.

vs.V, where a maximum of -7.5 V was applied. A linear relationship between these two parameters resulted to V = -5 V, indicative again of an abrupt junction. The intercept of this line with the x-axis represents the junction built-in potential, V_{bi}. From this curve

V_{bi} is ~ 2.0 V. This parameter can also be calculated from the equation [16]:

$$V_{bi} = \frac{kT}{q} \ln \left(\frac{n_{no} p_{po}}{n_i^2} \right) \qquad (3)$$

For this diode, the electron density on the n side at equilibrium (n_{no}) was ~ 4×10^{18} cm^{-3} and hole density on the p-side (p_{po}) was ~ 1×10^{17} cm^{-3}. The intrinsic carrier density (n_i) is 3 cm^{-3} in ß-SiC at 300K. With kT/q = .0259 V, the calculated value (V_{bi} = 2.07 V) and measured value of V_{bi} closely agree.

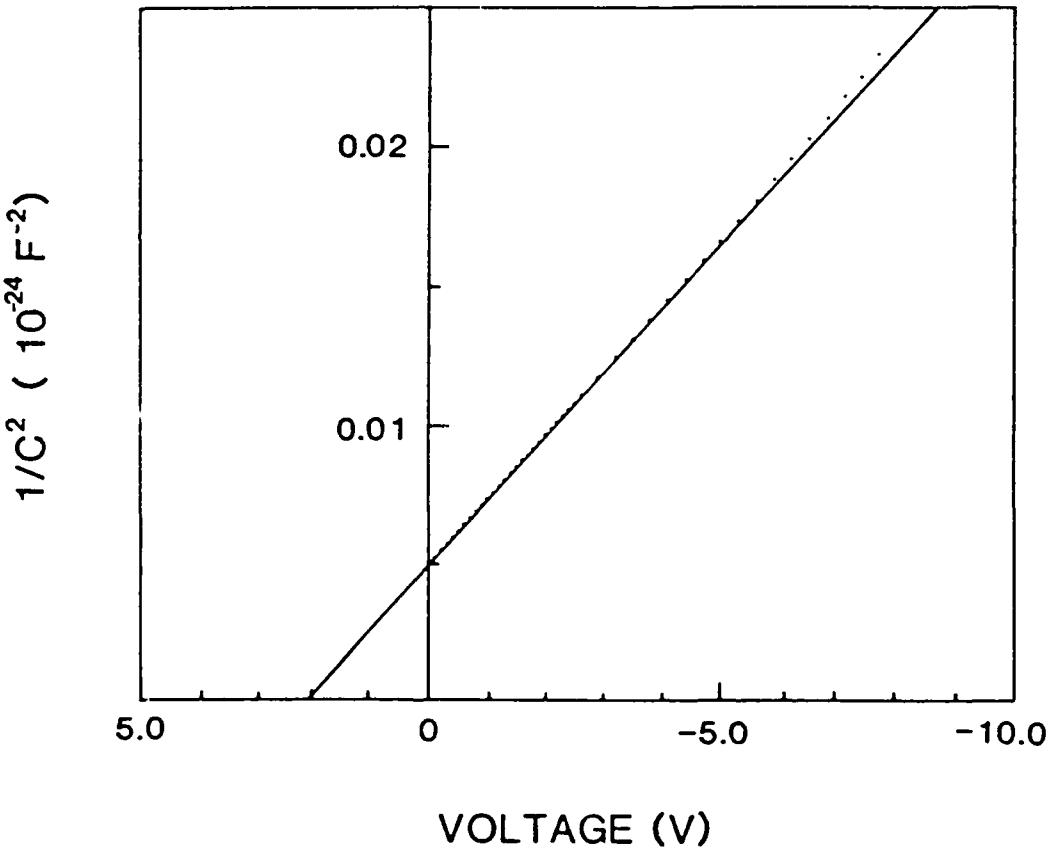


Fig. 5. Capacitance-voltage characteristics of diode in Fig. 1 at 300K.

b) Al-implanted Junctions

A similar analysis to that performed above was done on Al-implanted junctions. In this case, an acceptor specie (Al) was introduced into an unintentionally doped n-type ß-SiC substrate.

Figure 6 illustrates a typical linear plot of the I-V characteristics for this device up to a measurement temperature of 673K. The leakage current for a 300K measurement

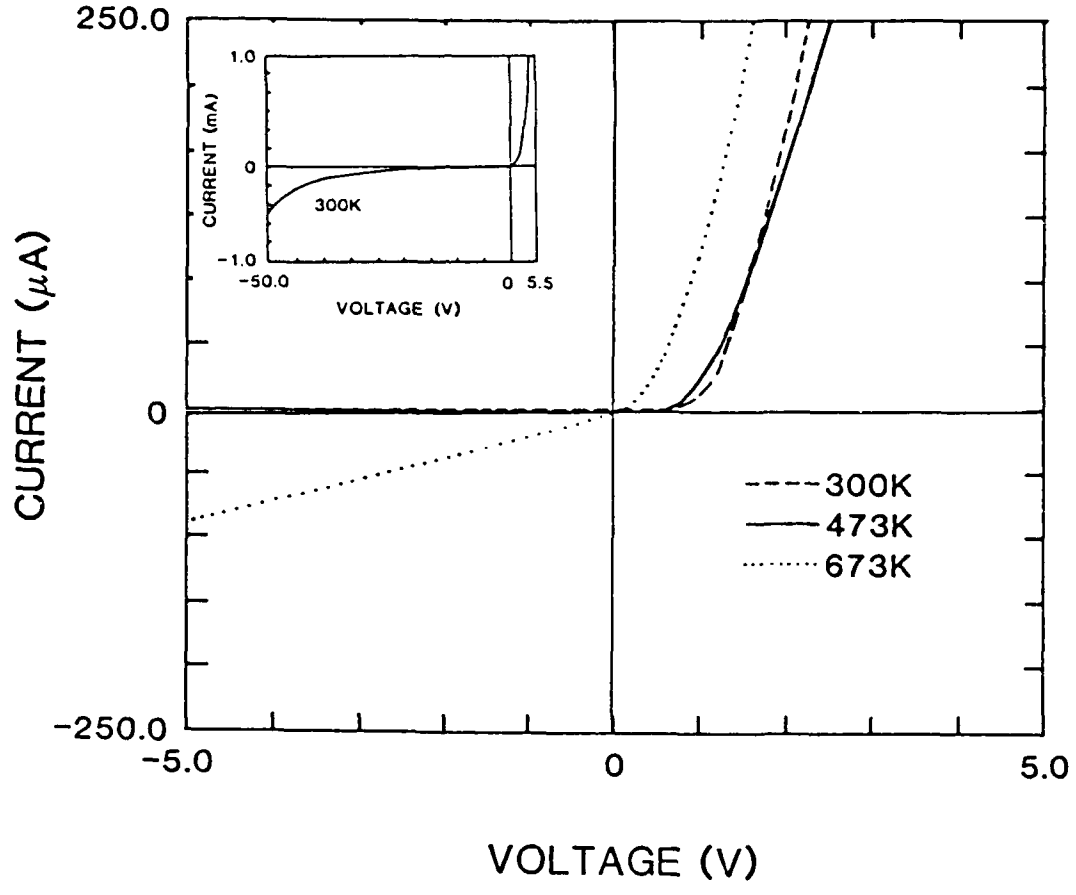


Fig. 6. Linear current-voltage characteristics for an Al-implanted junction diode in ß-SiC as a function of temperature.

was ~ 0.3 μA at -5 V. This increased to 500 μA at -50 V, as shown in the figure inset. At 473K, I_L increased only slightly to 85 μA at 673K. At room temperature, the forward

bias portion of the curve turned on at ~0.8 V. An increase in temperature reduced the turn on voltage. However, from the forward current results, it appears that the resistance of the device increased between 300K and 473K, decreasing again at 673K. This effect was not observed for the N-implanted diode.

Figures 7a and 7b show the log J-V characteristics of this diode between 300K and 673K in forward and reverse bias, respectively. In general, a hump in the current was observed at low forward bias (typically indicative of generation-recombination current in Si diodes [16]), followed by an exponential increase in current. However, the linearity of this latter region is not well defined, especially at higher temperatures. Estimates of the ideality factor for this device show an increase from 2.0 to 3.2 with increasing temperature. It appears that the current flow mechanisms dominating at low voltages obscure the conductance mechanism pertaining to the linear region observed best at low temperature. At higher voltages, there was no evidence of high-injection. However, the increase in resistance with temperature observed in Fig. 6 is clearly evident at 2.5 V in Fig.7a. As shown, the current decreased initially at 373K and then slowly increased with temperature to a value surpassing that obtained at 300K, at 673K. It is also important to note that the highest current obtained for this device was still a factor of 25 less than that obtained for the N-implanted diode.

Figure 7b illustrates the corresponding semilogarithmic plot for this diode in reverse bias. As previously observed, the reverse current increased with voltage. Again, current other than drift appears to dominate the reverse J-V properties of this diode. Likewise, the reverse current increased with temperature.

Logarithmic plots of the forward and reverse characteristics of this diode at 300K and 473K were also obtained (see Figs. 8a and 8b, respectively). As shown in Fig. 8a, the curve resulting at 300K is similar to the curve for N-implanted diodes at 473K shown

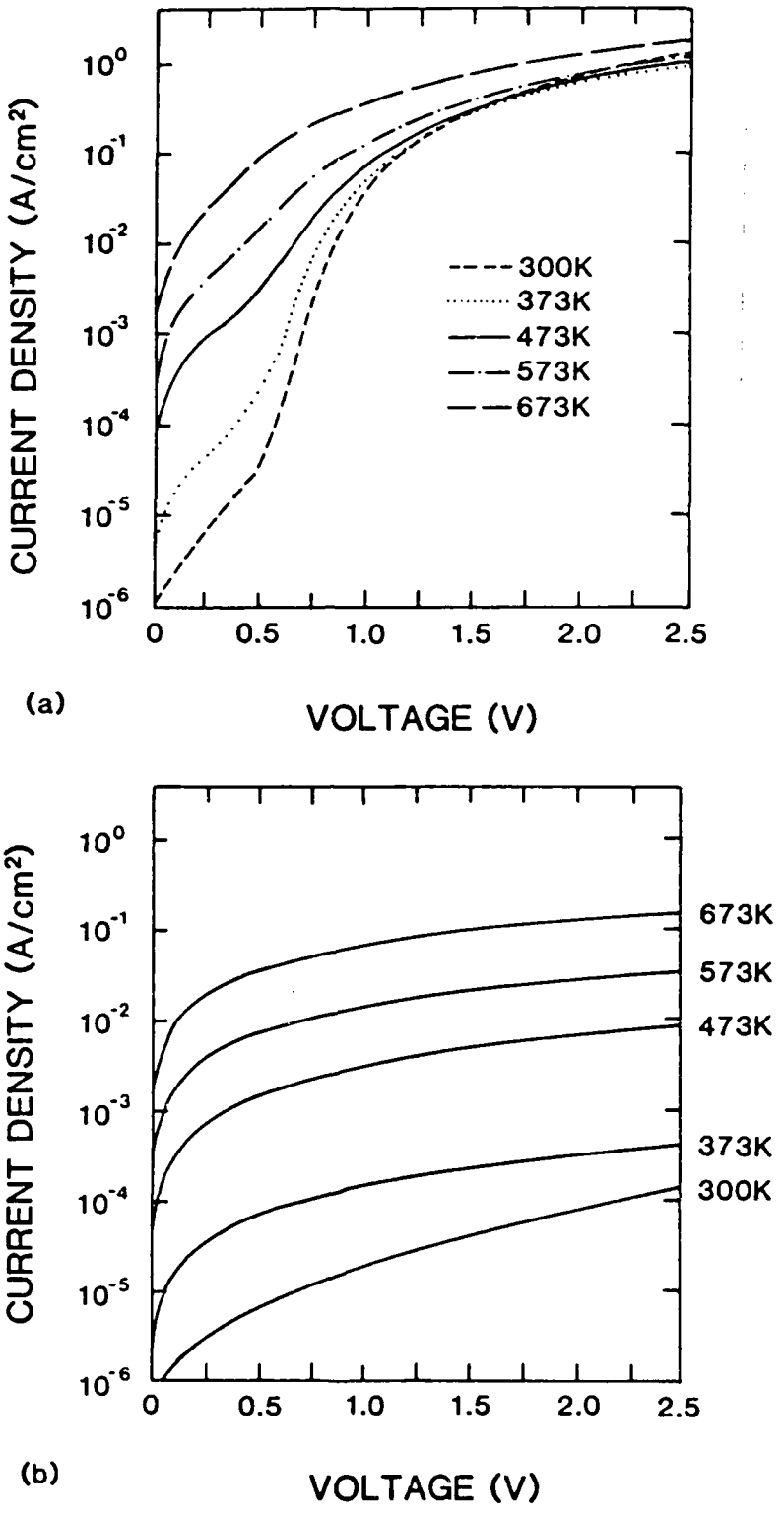


Fig. 7. Temperature dependence of log current density vs. voltage for diode in Fig. 6 under (a) forward and (b) reverse bias conditions.

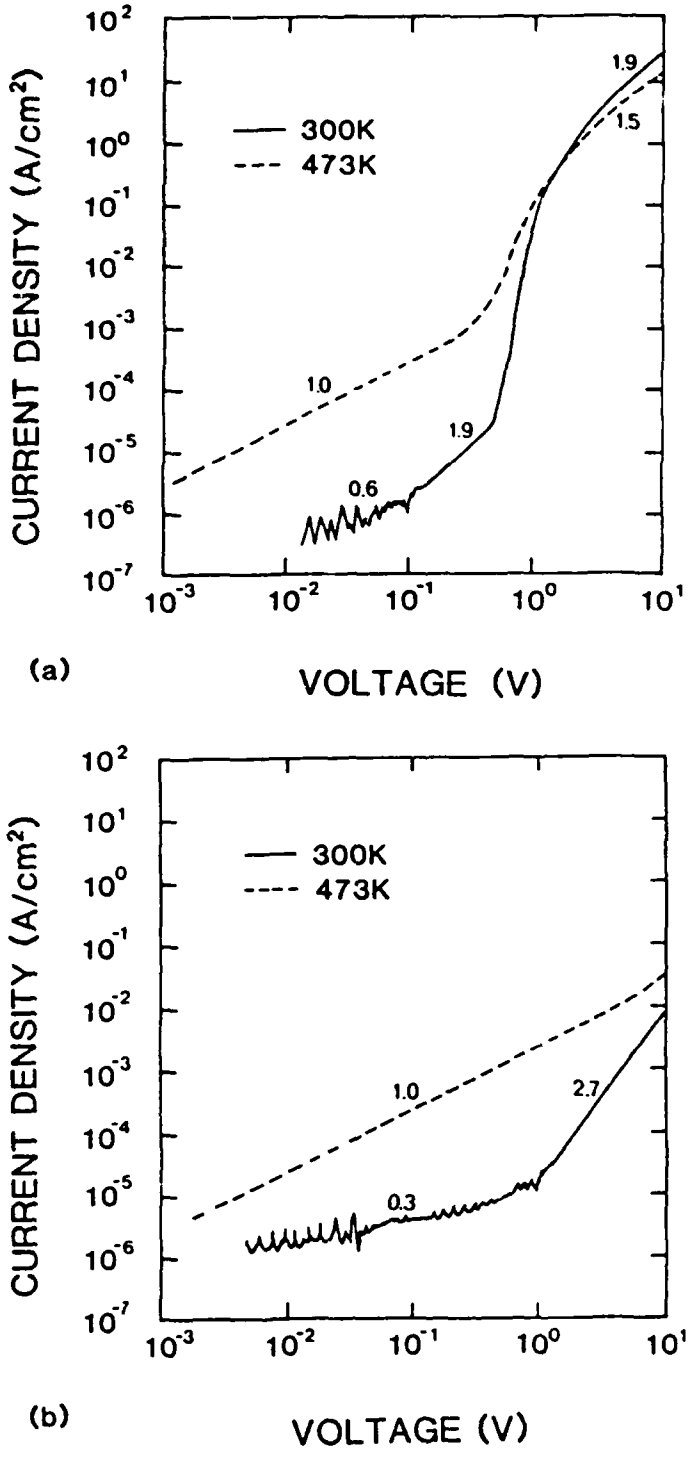


Fig. 8. Temperature dependence of log current density vs. log voltage for diode in Fig. 6 under (a) forward and (b) reverse bias conditions. Numbers on linear regions of curves denote the slope, m, where $J \propto V^m$.

in Fig. 3a. Initially, the current rose linearly with $J \propto V^{0.6}$. In the range $0.1\ V \leq V \leq 0.5V$ the current increased as $V^{1.9}$. Above 0.5 V, the current increased rapidly and became approximately linear again near 5 V where $J \propto V^{1.9}$. This again, is indicative of current conduction in an insulator. Upon heating to 473K, the shape of the log J - log V curve changed. From ~ 1 mV to ~0.2 V an ohmic relationship was observed. Current increased to a second linear region where $J \propto V^{1.5}$. As shown previously, the current in this region was lower at 473K than at 300K.

The corresponding reverse bias log J - log V plot is shown in Fig. 8b. At 300K, current increased as $V^{1/3}$ up to ~-0.6 V. This relationship is evidence that this diode is linearly graded as opposed to abrupt. At higher reverse biases (up to -10 V) the relationship $J \propto V^{2.7}$ was observed. At 473K, $J \propto V$ up to ~-3 V increasing to $J \propto V^{2.7}$ at the highest measurement voltage (-25 V not shown).

Figure 9 is a plot of log θ vs 1/T for this diode. This data was obtained from logJ-log V plots (in forward bias) between 313K and 373K. In this case, a trap energy and density of 0.22 eV and 2×10^{18} cm^{-3} respectively, resulted. The value of these parameters vary greatly with those obtained for N-implanted diodes.

Capacitance-voltage measurements were also performed on Al-implanted diodes. The capacitance values obtained were quite low, in the range $C \leq 2.5$ pF. Figure 10 shows a typical $1/C^2$ vs. V plot. A linear relationship up to ~-5 V resulted. This would indicate the junction is abrupt which conflicts with the low voltage reverse bias log J - log V results. In addition, V_{bi} from these C-V results was ~3.2 V, which is higher than the bandgap of ß-SiC.

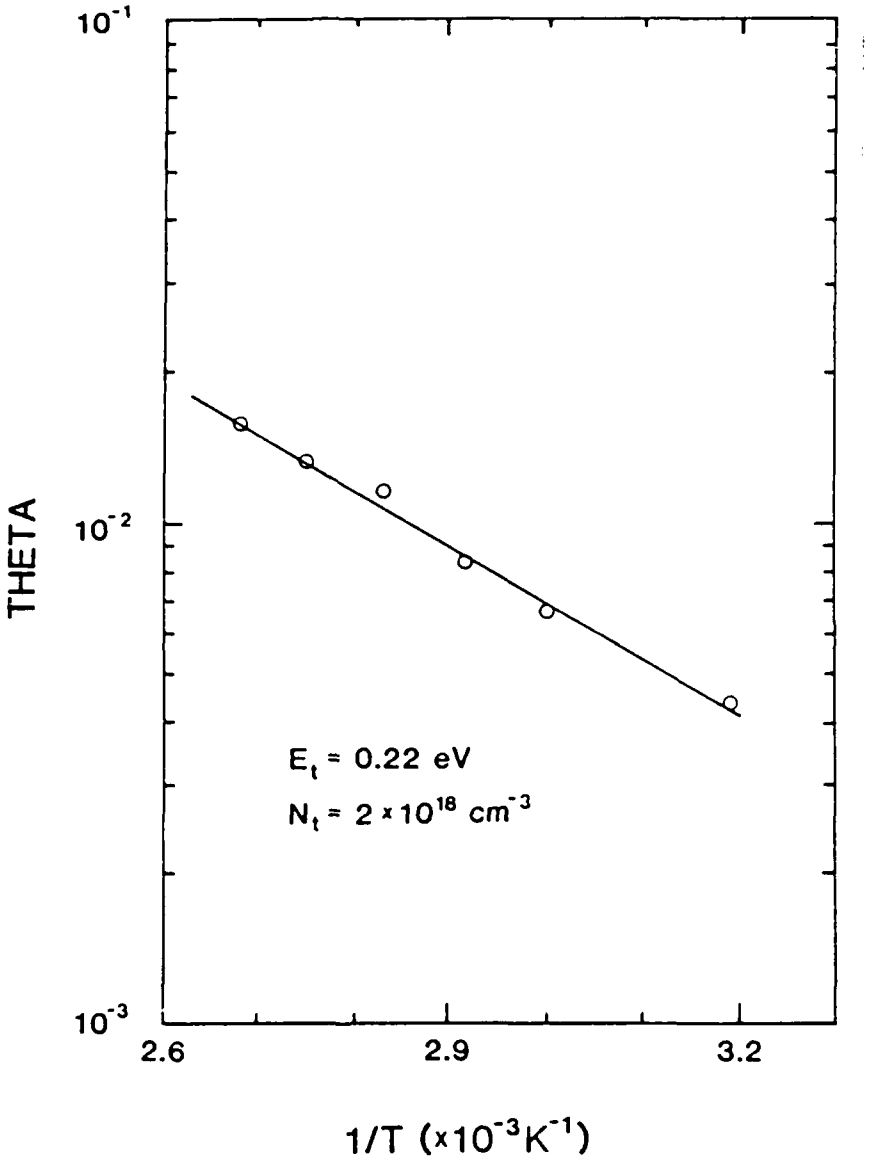


Fig. 9. Plot of log θ vs 1/T to determine trap energy and density in diode shown in Fig. 6.

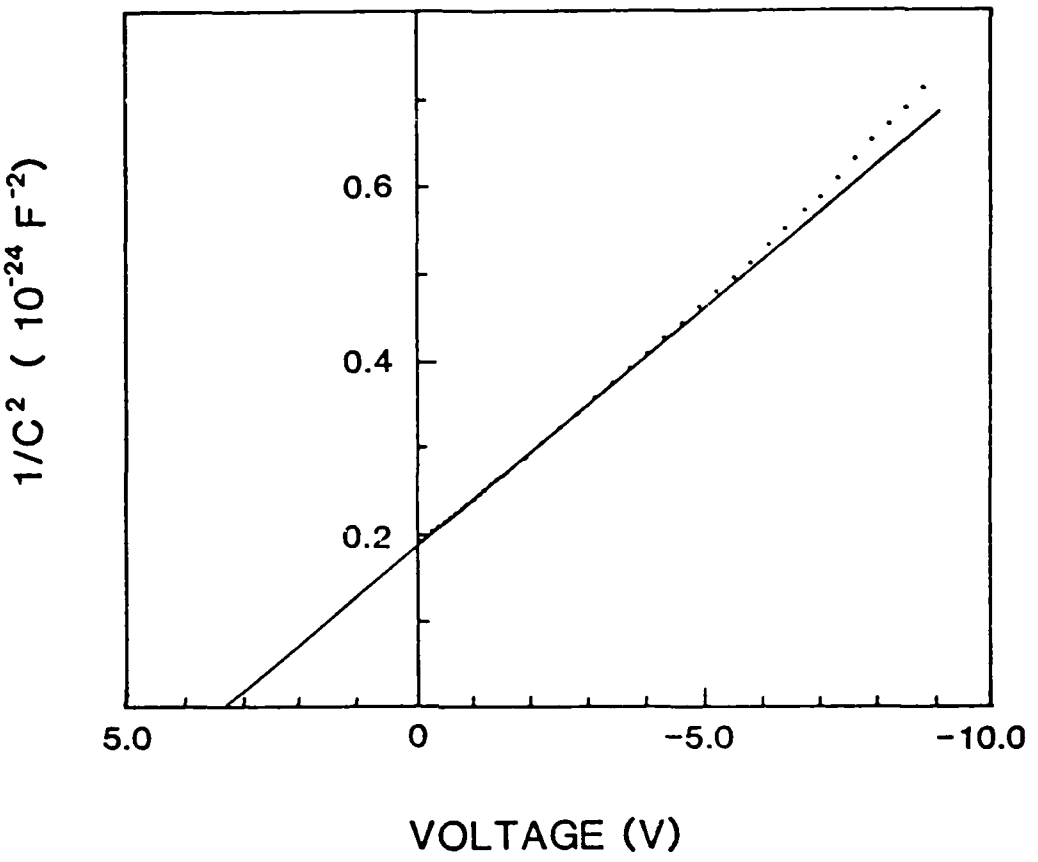


Fig. 10. Capacitance-voltage characteristics of diode in Fig. 6 at 300K.

DISCUSSION

a) Space-Charge-Limited Current

The linear I-V characteristics of ß-SiC junction diodes are qualitatively similar to those of standard semiconductor diodes. However, semilogarithmic plots of these characteristics yield an $n \approx 3$ for room temperature measurements. Similar values of n have also been reported for devices fabricated in β-SiC by Suzuki et al. [2] and in liquid-phase epitaxially grown 6H α-SiC by Ikeda et al. [17]. These jucntions were formed by introducing the dopant during growth. It has been suggested [17] that the

observed deviation from the normal semiconductor diode ideality factor in SiC devices is probably due to generation- recombination currents arising from deep trap levels contributed by defects near the junction interface. It should be pointed out, however, that diodes fabricated in α-SiC by ion-implantation of impurities [6], by in-situ doping of chemical vapor deposited layers [18] and junctions made in furnace grown crystals [19,20] yielded an $n \approx 2$ at room temperature. For temperatures approaching 673K, n in these devices approached 1. A detailed anlaysis of the logJ - logV plots of the diodes in the present research indicates space-charge-limited (SCL) current flow, as is the case with insulators and/or wide band-gap semiconductors.

Space-charge-limited current flow in solids has been considered in detail by Lampert and Mark [13]. They loosely defined materials with $E_g \leq 2$ eV as semiconductors and those with $E_g \geq 2$ eV as insulators. Beta-SiC could be considered as a borderline case, since $E_g = 2.2$ eV. This current flow mechanism typically observed in insulators, has been reported in 6H α-SiC [19,21]. Additionally, SCL current flow has been observed in GaAs [22], high resistivity [23] and amorphous [24] silicon and germanium [25].

For the purpose of illustration of this phenomenon in such materials, consider the four log I vs. log V graphs in Fig. 11. Figure 11(a) represents an ideal insulator where $I \propto V^2$, indicating SCL current flow. In other words, there are no thermally generated carriers resulting from impurity-band or band-to-band transitions; the conduction is only within the conduction band as a result of carrier injection. As shown in Fig. 11(b), ohmic conduction is obtained in trap-free insulators in the presence of thermally generated free carriers, n_o. When the injected carrier density, n_{inj}, exceeds n_o ($n_{inj} > n_o$), ideal insulator characteristics are observed ($I \propto V^2$). Shallow traps contribute to an $I \propto V^2$ regime at a lower voltage followed by a sharp transition to an ideal insulator, square-law regime as

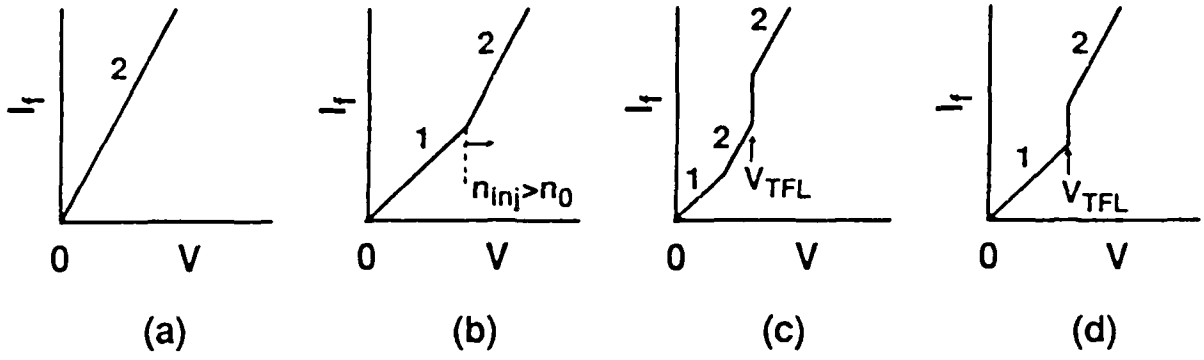


Fig. 11. Schematic drawings of the logarithmic dependence of current versus voltage for (a) an ideal insulator, (b) a trap free insulator with thermally generated free carriers, (c) an insulator with shallow traps and thermal free carriers and, (d) an insulator with deep traps and thermal free carriers.

shown in Fig. 11(c). The sharp transition corresponds to an applied voltage, V_{TFL} (TFL≡trap-filled-limit) required to fill a discrete set of traps which are initially unoccupied. Figure 11(d) illustrates the case of a material with deep traps which have become filled when n_{inj} becomes comparable to n_0. The voltage at which this occurs is V_{TFL}. Therefore, at $V < V_{TFL}$ ohmic conduction is observed and at $V > V_{TFL}$ SCL current flow dominates.

The ß-SiC junction diodes used in the present study show all the I-V regimes discussed above, though not all in the same diode at a single measurement temperature. Temperature influences the occupation probabilities of the various trap levels and the degree of impurity ionization, thereby causing a transition from either shallow to deep or deep to shallow trapping as observed in the logarithmic plots of forward characteristics as a function of temperature. However, before further discussion of results, it is important to note the following observations.

From examination of the semilogarithmic plots shown in Figs. 2(a) and 7(a), it becomes apparent that a portion of the characteristic curves is indeed exponential in nature. This exponential regime can be fitted to the diode equation, Eq. 1 above, with n typically greater than 2.0, although SCL current flow may well be the dominant conduction mechanism. In fact, these linear regions observed in the semilogarithmic plots, correspond to the voltage range where the onset of the sharp rise in current is observed in the corresponding logarithmic plots shown in Figs. 2(b) and 7(b). The current in the upper portion of these curves, where $I \propto V^{\sim 2}$, indicative of SCL current, may also be influenced by high-level injection and series resistance effects. These effects are likely to degrade the $I \propto V^2$ power law. Indeed, high-level double injection of carriers which yields $I \propto V^{1.5}$ [26] may contribute to the observed device characteristics.

b) Forward Bias Characteristics

Deep trapping was observed at a measurement temperature of 300K for the N-implanted junction previously presented (see Fig. 3a). Between 300K and 473K, a transition from deep to shallow trapping occurred. From the plot of θ vs. 1/T, obtained in the shallow trapping regime, a trap energy and density of 0.55 eV and 2×10^{16} cm^{-3}, respectively, were determined. It is believed that this trap is an acceptor level located 0.55 eV above the valence band edge which contributes to deep-electron trapping when electrons constitute the major proportion of the injected carrier density, i.e. at lower temperature ($\leq$423K) in the n^+-p junction. The same trapping center when occupied by electrons may contribute to shallow trapping of holes upon substantial hole injection; this would occur at higher operation temperatures ($T \geq 423K$). Experimentally these effects, i.e. deep trapping and shallow trapping at low and high temperatures, respectively, are observed. However, the assumption that this trap level is an acceptor level and 0.55 eV above the valence band rather than 0.55 eV below the conduction band, is based on two

experimentally observed results regarding the electronic nature of our material.

Segall et al. [27], performed Hall measurements on many n-type ß-SiC thin films. Their conclusion was that this material contains, intrinsically, a compensating acceptor species. The present authors believe the above trap is that compensating entity. However, the origin of this trap is unknown. Secondly, work by Nagesh et al. [28], regarding deep level transient spectroscopy on these same films, indicated the absence of traps in the upper one-third of the band gap (0.73 eV). Since 0.55 eV falls within this range, a logical conclusion would be that the trap is above the valence band by this energy value.

The opposite effect of temperature on the type of trap operating was observed in the Al-implanted p^+-n junction. At temperatures below ~423K, injected holes, which are the dominant carriers, are believed to be shallow trapped by centers with a density and energy of $2x10^{18}$ cm^{-3} and 0.22 eV, respectively, and located above the valence band edge. It appears that this shallow level is contributed by occupied Al acceptor centers which have been determined to have an ionization energy of 0.216 eV [29] in β-SiC. From the implant conditions and this ionization energy, the maximum ionized carrier density is calculated to be ~$7x10^{17}$ cm^{-3}. The value of both these parameters are very similar to what was obtained from the θ vs 1/T plot for this diode.

At temperatures above ~423K, the forward log J - log V characteristics indicated deep-level dominated conduction. This level is believed to be the shallow level observed in the n^+-p junction previously discussed.

Finally, it is important to note a finding by Zhou et al. [30] regarding traps in ß-SiC. Contrary to Nagesh et al. [27], these investigators reported the presence of two trap levels 0.34 eV and 0.68 eV below the conduction band as determined by DLTS on ß-SiC Schottky barrier diodes. They attributed the latter trap to interface defects formed via high-temperature oxidation. The origin of the former was not known. The presence of

these traps are not reflected in the present I-V measurements. However, I-V characteristics of Schottky barrier diodes are presently being studied in our laboratory to determine the presence of majority carrier traps.

c) Reverse Bias Characteristics

From the dependence of the reverse current densities (J_r) on low reverse biases (V_r), $J_r \propto V^{1/2}$ in n^+- p and $J_r \propto V^{1/3}$ in p^+-n diodes, it appears that generation processes dominate at low voltage. For the generation process to dominate, there must be allowed states in the band-gap. A detailed study of J_r - V_r was not carried out, as measurements at low biases were unreliable due to noise. However, this observation is an indication that surface leakage currents are minimal. The states operational in the reverse bias generation process could well be the same trap-states observed in the forward bias characteristics. At higher biases, an ohmic dependence of current on voltage was observed. At even higher biases $J \propto V^n$, where n was between 2 and 6. Similar observations were reported by Patrick [19] in α-SiC junctions. He interpreted the ohmic regime as conduction through a high resistivity intrinsic layer sandwiched between the p and n regions of the junction. A similar layer was also considered to exist by Marsh and Dunlap [6] in their interpretation of the observed electrical characteristic of implanted junctions in α-SiC. In the present diodes, there was no indication of the presence of a high resistivity layer.

The C-V measurements indicated an abrupt junction in both types of [illegible] although reverse J-V characteristics results indicated a graded junction in the [illegible] case. The reason for this discrepency is not clear. However, [illegible] measurements, it appears that the ohmic region observed [illegible] manifestation of a complex generation process providing [illegible] Furthermore, the region where $J \propto V^2$ (beyond the ohmic [illegible] conduction. A power law with $n > 2$, as was [illegible]

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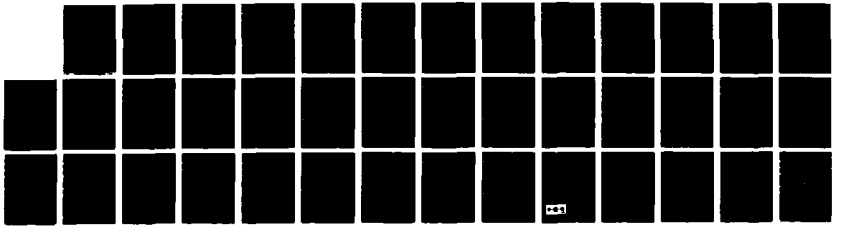

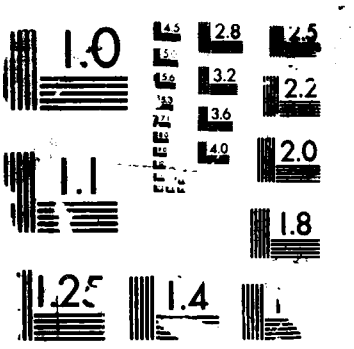

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presence of a uniform distribution of traps in the band [13]. This situation is not visualized in the present ß-SiC diode where only discrete levels are evident from the forward J-V characteristics. Therefore, a regime where $J \propto V^6$ is probably an indication of localized avalanche breakdown.

CONCLUSIONS

The I-V characteristics of N-implanted (n^+-p) and Al-implanted (p^+-n) junction diodes fabricated in ß-SiC showed rectification up to a temperature of 673K. These characteristics have been interpreted qualitatively in terms of SCL current in the presence of shallow and deep traps. Two trap-levels appear to be present: (1) 0.55 eV and (2) 0.22 eV above the valence band edge. The 0.55 eV level has a concentration of 2×10^{16} cm^{-3}; these probably account for the compensating centers present in the material. The shallower of the two trap levels has a concentration of 2×10^{18} cm^{-3}. This appears to be ionized Al centers present in the depletion region of the Al implanted p^+-n diodes. The contribution and the nature of the trapping process of a particular center arises from its charge state and occupation probability as determined by the position of the quasi-Fermi levels in the depletion layer.

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VIII. ELECTRICAL CONTACTS TO BETA SILICON CARBIDE THIN FILMS

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ABSTRACT

Ohmic and rectifying electrical contacts to n- or p-type semiconducting β-SiC thin films were developed and characterized. Upon annealing for 300 s at 1523K, Ni, Au-Ta and Cr were ohmic on n-type material. $TaSi_2$, similarly heated to 1123K, and as-deposited Al also showed ohmic character. $TaSi_2$ had the lowest room temperature contact resistivity of 2.0×10^{-2} Ω-cm^2. For p-type β-SiC, Al-$TaSi_2$ annealed for 1800 s at 1473K and Al annealed for 180 s at 1150K exhibited ohmic behavior. Al was the better of the two, having a room temperature contact resistivity of 3.1×10^{-2} Ω-cm^2. High temperature measurements of Al and $TaSi_2$ contacts showed that these contacts are stable during electrical operation to at least 673K for eight hours in air. At this temperature the contact resistivity of $TaSi_2$ and Al on β-SiC decreased by a factor of two and ten, respectively. Contacts of Au were shown to be rectifying on n-type β-SiC with a barrier height of 1.20 eV.

INTRODUCTION

Monocrystalline silicon carbide (SiC) is currently being produced and studied throughout the world for use as the material host for future electronic devices in specialized high temperature, high frequency, high power and optoelectric applications. It occurs in both a single cubic polytype (also referred to as β-SiC*), as well as numerous alpha polytypes which are either hexagonal or rhombohedral in structure. The β form is believed to be the most promising for electronic applications due to its smaller band gap (2.2 eV vs. 2.86 eV for the most common α polytype of 6H*) and its higher theoretical saturation electron drift velocity. Significant advances in recent years by several investigators (e.g., see Refs. 1-8) regarding the chemical vapor deposition of β-SiC on Si substrates, have allowed high purity thin films to be obtained. However, to exploit the full potential of this material for electronic applications, reliable ohmic and rectifying contacts are essential.

Several metallic elements (e.g., W, Mo, Cr, Ni) and alloys (e.g., Au-Ta, Au-Ta-Al, W-Mo, Cr-Ni, Cu-Ti, Al-Si) have been developed as ohmic contacts for α-SiC (9-13); however, no information on the contact resistivity of these materials was reported. For the majority of the contact materials noted above, annealing temperatures exceeding 2000K were required to achieve ohmic character. This temperature treatment often results in deep penetration of the deposited contact material which can cause electrical shorting of devices. Moreover, the success of these contacts on hexagonal, α– SiC does not necessarily guarantee that they will be suitable for the cubic, β form. In the case of the latter material, as-deposited and annealed Al have been shown (14) to be ohmic on n-type and p-type material, respectively. Again, no values of the contact resistivities were reported. Finally, in no case has the dependence of the contact resistivity on operating

*Beta SiC is also frequently denoted as 3C which refers to the fact that three closest packed layers of SiC_4 tetrahedra are required to produce periodicity in the cubic (C) material. Similarly, the 6H notation refers to the six closest packed layers of tetrahedra necessary to build the hexagonal (H) unit cell.

temperature been determined for ohmic electrical contacts on any polytype of SiC.

Schottky contacts on SiC are also of great interest because they are relatively immune to the speed limitations associated with minority carrier storage in p-n junction devices. Thus, for high frequency applications, rectifying contacts are very important. This is especially true in SiC, where the known acceptor levels are sufficiently deep (i.e., 0.26 eV for Al and 0.73 eV for B) that high concentrations of impurity doping are required to obtain p-type layers. This results in low hole mobility in the p layers and a poor quality p-n junction.

Previous work involving rectifying contacts on SiC has been somewhat inconclusive. Rectifying contacts of Al, Ag and Au on 6H-α-SiC were reported (15, 16) to have barrier heights of approximately 1.45 eV. These values were also reported to be independent of the work function (4.25, 4.36 and 4.46 eV, respectively) of the metal used. Two studies have been reported regarding rectifying contacts on β-SiC. Verenchikova et. al. (17) determined the barrier heights of as-evaporated Cr (work function = 4.38 eV) as a function of the polytype for several α-SiC crystals using capacitance-voltage (C-V) and photoresponse methods. An analogous value for β-SiC could not be measured; however, a value was obtained by extrapolation of the data from the other polytypes to zero percent hexagonality. The reported values were 1.1-1.2 eV and 0.4 eV on 6H- and β-SiC, respectively. The lower barrier height for Cr on β-SiC was attributed to a high density of C vacancies at the material surface. In a separate study, Yoshida et. al.(18) examined Au contacts on chemically etched n-type β-SiC also using C-V and photoresponse techniques. In this case, the barrier height was reported to be approximately 1.15 eV. Thus, in contrast to the case of rectifying contacts on 6H-SiC, the barrier height of this type of contact on β-SiC appears to depend on the work function of the metal species. Studies to address this controversy were undertaken in the early stages of this research program using Cr and Au as the contact materials.

The objectives of the present research were the determination of (1) the contact resistivities of some of the materials commonly used and newly developed for contacts on β-SiC, (2) the operation temperature dependence of the contact resistivities of Al and $TaSi_2$ on p- and n-type β-SiC, respectively and (3) the barrier height of the Schottky contact of Au on β-SiC. The following sections describe the experimental procedures used to achieve these objectives and discuss the results obtained.

EXPERIMENTAL PROCEDURES

The monocrystalline thin films of β-SiC used in the present research were grown at 1630K-1 atm. total pressure on Si(100) substrates via two-step chemical vapor deposition (CVD) using SiH_4 and C_2H_4 entrained in flowing H_2. The as-grown, unintentionally doped samples were invariably n-type. Samples having p-type character were produced by doping with Al during growth. The growth and doping procedures have been described in detail elsewhere (7, 8, 19). The as-grown films were polished with 0.1 μm diamond paste to remove the 100-200 nm surface roughness and to eliminate possible surface defects introduced during the final stages of growth. This procedure removed approximately 300 nm of material from the SiC surface. After polishing, the samples were immersed in H_2SO_4 for five minutes at 433K-453K, rinsed in deionized (DI) water, soaked in a 1:1 mixture of NH_40H and H_20_2 for five minutes at 333K-343K, rinsed in DI water, etched in buffered HF for two minutes and rinsed in DI water at least five times. Immediately after cleaning the samples were oxidized at 1473K in dry 0_2 for 1.5 hours in order to remove polishing -induced surface damage and residual contaminants. During oxidation, approximately 100 nm of SiO_2 formed which corresponds to the removal of approximately 40 nm of SiC. This oxide was then removed by a brief immersion in HF.

Following the cleaning procedure described above, samples, other than those on which contacts of $TaSi_2$ were to be placed, were mounted in a vacuum evaporator which

was subsequently evacuated to a base pressure of 1 x 10^{-6} Torr. The n-type ohmic and rectifying contacts of Al, Ni or 97 a/o Au-3 a/o Ta and Au or Cr (Cr was subsequently determind to be ohmic), respectively, and the p-type ohmic contacts of Al or 91 a/o Au-2 a/o Ta - 7 a/o Al were individally deposited by thermal evaporation from a W-boat. Tantalum silicide ($TaSi_2$), another n-type ohmic contact material, was deposited via rf sputtering of a $TaSi_2$ target. The thickness of each of these contacts was approximately 250 nm. An additional p-type ohmic contact was prepared by depositing 50 nm of Al by thermal evaporation, followed by sputtering a 250 nm covering layer of $TaSi_2$. Following deposition, circular contacts with an area of 3.14 x 10^{-4} cm^2 were delineated on all samples using photolithographic techniques. Contacts for Schottky diodes were fabricated using the techniques noted above. Specifically, Au or Cr were deposited for the rectifying contacts while sputtered $TaSi_2$ was employed as the ohmic contact material.

Ohmic contacts to β-SiC samples were annealed at various temperatures (see "Results and Discussion") in vacuum (10^{-6} - 10^{-5} Torr) or, in the case of Al, a 0.3 Torr flowing Ar atmosphere to obtain electrically stable contacts. Current-voltage (I-V) characteristics were then measured using an HP 4145A semiconductor parameter analyzer and a probe station equipped with a hot stage open to air. Contact resistance values were determined by both the three contact (20) and extrapolation (21) method and converted to contact resistivities by multiplying these values by the contact area. In the former method, the spacing between the closest and furthest set of contacts was 500 μm and 2600 μm, respectively. In the latter method, the contact spacing was 500 μm. In each case, the current was kept low (100 μA) in order to avoid sample heating during measurements. Following the annealing procedure above, the same instrumentation with a hot stage attachment to the probe station was utilized to measure the change in contact resistivity values with varying operation temperature.

The I-V characteristics of Schottky diodes were measured using the instrument noted above. The bias was swept from -100V to 5V in order to deduce the quality of the diodes. The C-V character of these rectifying contacts was measured at 1 MHz and displayed with a PAR 410 C-V plotter. From the C-V curve, the relationship between $1/C^2$ vs. V was obtained.

RESULTS AND DISCUSSION

Ohmic Contacts

a. n-type β-SiC

Of the contacts made to n-type β-SiC in this research, as-deposited Ni, Au-Ta, $TaSi_2$ and Cr exhibited nonlinear I-V characteristics; however, the resistivity to current flow in either voltage direction was small, as seen in the representative curve for as-deposited $TaSi_2$ shown in Fig. 1. Conversely, as-deposited Au contacts were very rectifying as will be subsequently shown. Hereafter, Cr, which was considered for its rectifying properties on β-SiC at the start of these experiments, will be discussed for its ohmic behavior.

Contact resistivity values for n-type β-SiC (carrier concentration ~ 5×10^{16} cm^{-3}) are listed in Table I†. Prior to each measurement, the Ni, Cr and Au-Ta contacts were independently heated for 300s to 1523K; the $TaSi_2$ contact was similarly heated to 1123K. The contact resistivityvalue for Al is for as-deposited material. The $TaSi_2$ contact had a slightly lower resistivity than the other contacts. Furthermore, it was observed that its contact resistivity was not significantly changed with annealing temperatures above 1123K (the maximum annealing temperature for this contact material was 1473K). Thus, reproducible and moderatley low resistivity ohmic contacts may be obtained on n-type

†contact resistivity values obtained using both the extrapolation and three contact method were typically within 25% of each other. For breavity, only those values obtained using the extrapolation method are given in Tables I-IV.

Table I. Contact resistivities of Al, Ni, Cr, Au-Ta and $TaSi_2$ on n-type β-SiC having a carrier concentration of 5×10^{16} cm^{-3}

Materials	Contact Resistivity (Ω-cm^2)
Al	1.6×10^{-1}
Ni	1.4×10^{-1}
Cr	7.0×10^{-2}
Au-Ta	3.0×10^{-2}
$TaSi_2$	2.0×10^{-2}

β-SiC by rf sputtering of $TaSi_2$ coupled with thermal annealing. As such, this material will be the principal focus of the following discussion regarding ohmic contacts on this material.

The nonlinear I-V characteristics previously noted and shown in Fig. 1 for the as-deposited $TaSi_2$, became linear upon annealing at 1123K for 300s. The same effect was observed when heating the Ni, Cr and Au-Ta contacts to 1523K. Thus, thermal annealing of these contact materials on SiC was required to achieve operational ohmic character and to minimize contact resistivity.

In contrast to the above results, Al (a common p-type dopant in SiC) evaporated onto n-type β-SiC showed ohmic behavior in the as-deposited state. However, upon heating to 1173K for 180-300 s, this contact became rectifying. Daimon et. al. (14), have recently published similar results showing that the rectifying properties are caused by the diffusion of the Al into the β-SiC and the resultant formation of an alloyed p-n junction.

The operation temperature dependence of the contact resistivity for $TaSi_2$ is given in Table II. Heating this combination of materials to as high as 573K did not significantly alter the contact resistivity. However, upon heating this sample to 673K, this value decreased and the ohmic character of the contacts improved. This is illustrated in the I-V

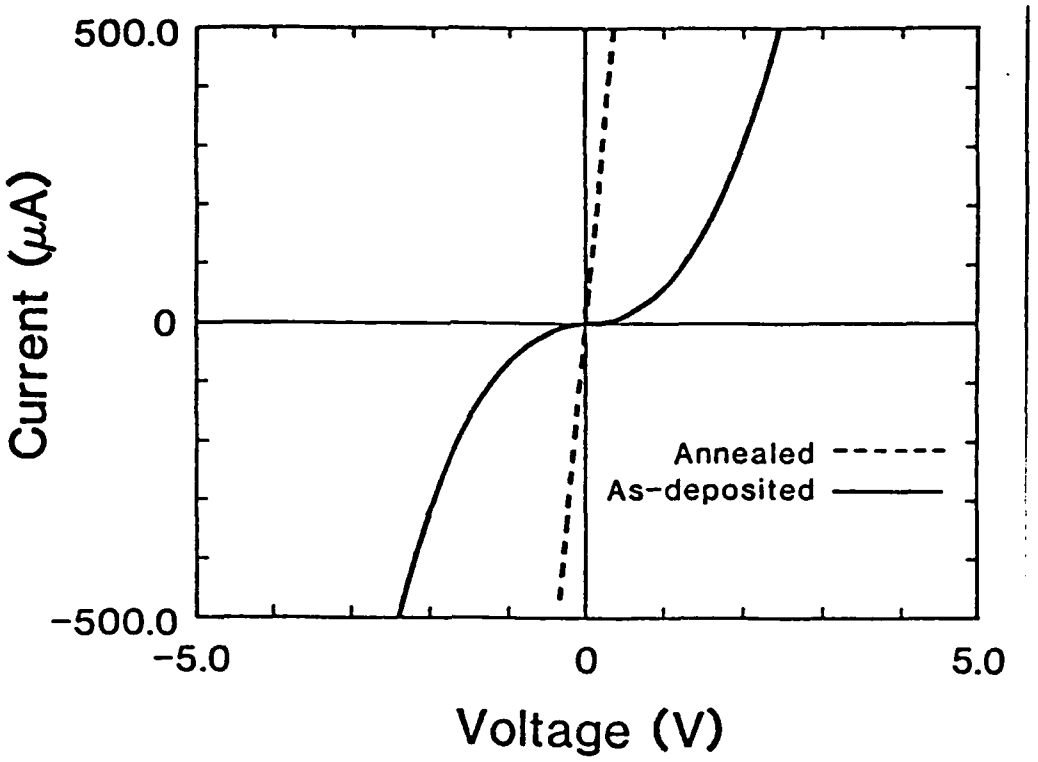

Fig. 1. Room temperature I-V plot showing ohmic contact properties of rf-sputtered $TaSi_2$ on n-type β-SiC (a) as deposited and (b) annealed at 1123K - 300 s in vacuo.

plot shown in Fig. 2. A decrease in contact resistivity with increasing temperature is expected, since the carrier concentration in the material is increasing in this temperature range (22). However, it is not presently understood why a decrease is not observed when heating from 298K up to 573K. It is important to note that the process of decreasing and increasing contact resistivity with temperature was reversible through many heating and cooling cycles. This discounts the possibility of any additional solid state reactions between the contact material and semiconductor beyond which may have occurred during the initial high temperature annealing.

Table II. Change in contact resistivity with temperature for $TaSi_2$ on n-type β-SiC

Temperature (K)	Contact Resistivity (Ω - cm^2)
298	2.0×10^{-2}
373	2.1×10^{-2}
473	2.2×10^{-2}
573	1.8×10^{-2}
673	9.6×10^{-3}

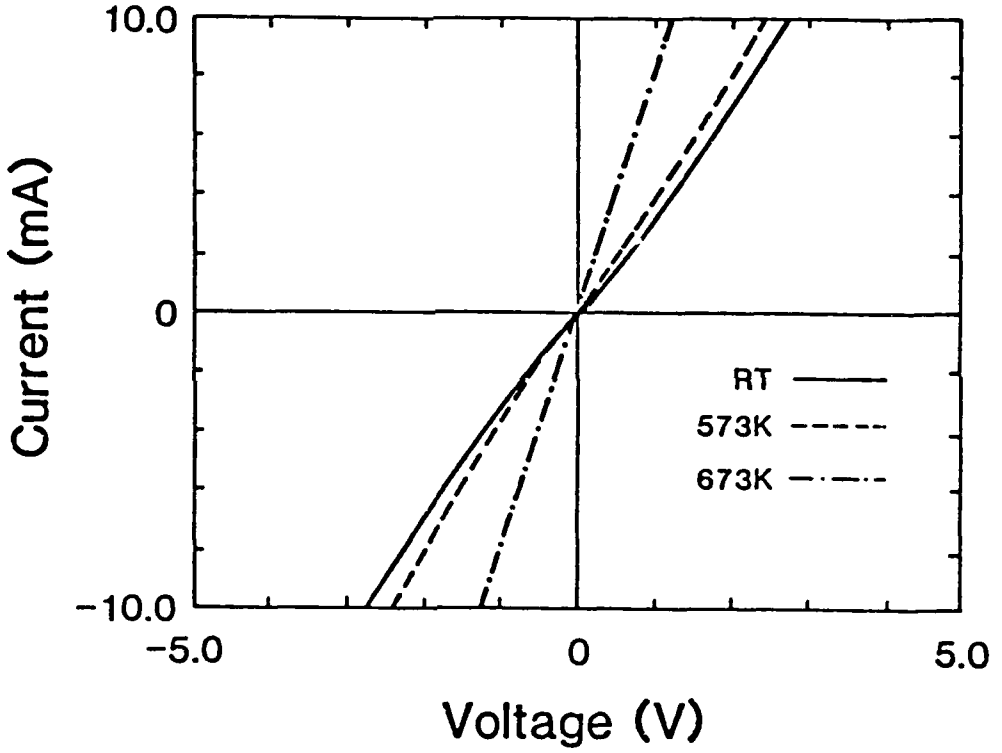

Fig. 2. Operation temperature dependence on ohmic contact properties of rf-sputtered $TaSi_2$ on n-type β-SiC. (a) Room temperature, (b) 573K and (c) 673K results.

b. p-type β-SiC

Aluminum, a 91 a/o Au - 2 a/o Ta - 7 a/o Al alloy and the special Al/$TaSi_2$ alloy described previously were examined for ohmic behavior on p-type β-SiC (Al doped, carrier concentration ~ 1×10^{16} cm^{-3}). Table III summarizes the contact resistivity values

Table III. Contact resistivity of Al, Au-Ta-Al and Al-$TaSi_2$ on p-type β-SiC ($p \approx 1 \times 10^{16} cm^{-3}$)

Material	Contact Resistivity (Ω - cm^2)
Au-Ta-Al	4.7×10^{-1}
Al-$TaSi_2$	2.0×10^{-1}
Al	3.1×10^{-2}

obtained for these three materials. Even after heating at 1473K for 1800 s, the Au-Ta-Al alloy contact showed nonlinear I-V characteristics and possessed a high contact resistivity (~ 4.7×10^{-1} Ω - cm^2). Thus it was unsuitable as an ohmic contact. By contrast, contact resistivity for the Al/$TaSi_2$ combination was measured to be 2.0×10^{-1} Ω - cm^2 after a 1473K, 1800 s anneal. (This contact exhibited very poor, non linear behavior after heating at 1073K for 1800 s). Thus, although linear I-V behavior was observed, the resistivity of this contact was rather high.

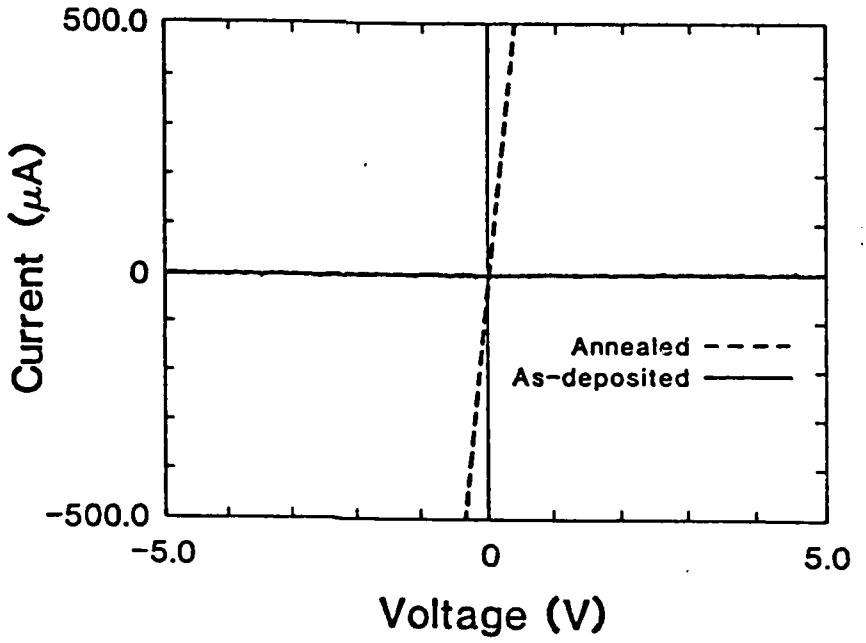

Fig. 3. Room temperature I-V plot showing ohmic contact properties of evaporated Al on p-type β-SiC (a) as-deposited and (b) annealed at 1150K for 180 s in .3 T flowing Ar.

Annealed Al was also utilized as an ohmic contact on p-type β-SiC. As-deposited this contact had a very high resistivity. After heating to 1150K for 180 s, the contact was ohmic with a resistivity of 3.1×10^{-2} Ω - cm^2. This is illustrated in the I-V plot shown in Fig. 3. It is speculated that annealing at 1150K results in a very shallow p+ region under the contact area created by Al diffusion into the p-type β-SiC. Further annealing to temperatures as high as 1273K did not result in any measurable decrease in contact resistivity from the 1150K value.

The temperature dependence of contact resistivity for Al on p-type β-SiC is summarized in Table IV. In every instance, an increase in measurement temperature resulted in a decrease in the contact resistivity. This phenomenon was also reversible, i.e., cooling from 673K to 298K resulted in an increase of the contact resistivity from 2.2×10^{-3} to 3.1×10^{-2} Ω -cm^2. Figure 4 shows the linearity of these contacts at the various measurement temperatures. No change was observed in the shape or slope of any of these curves or those shown for $TaSi_2$ in Figure 2 with time (for periods up to eight hours). This demonstrates the usefulness of this contat material on p-type β-SiC at elevated temperature.

Table IV. Change in contact resistivity with temperature for Al on p-type β-SiC

Temperature (K)	Contact Resistivity (Ω - cm^2)
298	3.1×10^{-2}
373	1.4×10^{-2}
473	6.3×10^{-3}
573	3.3×10^{-3}
673	2.2×10^{-3}

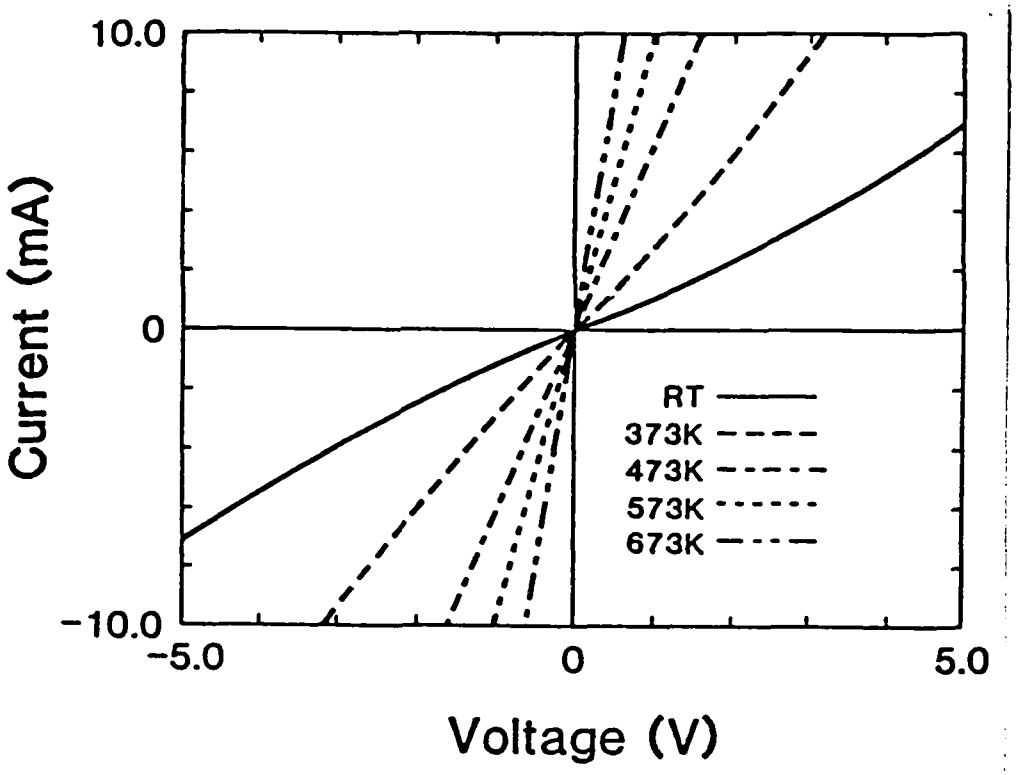

Fig. 4. Operation temperature dependence on ohmic contact properties of evaporated Al on p-type β-SiC. (a) Room temperature, (b) 373K, (c) 473K, (d) 573K and (e) 673K results.

Schottky Barrier Contacts

Schottky barrier diodes composed of Au rectifying and $TaSi_2$ ohmic contacts were produced on the n-type β-SiC films. Figure 5 shows a typical I-V curve of such a diode on a film with a carrier concentration of 9×10^{15} cm^3. Although the leakage current increased with applied reverse bias, breakdown did not occur within the applied voltage limits of the I-V measurement system (-100V). The diode ideality constant, n, was determined to be 2.1 from the log current vs. forward bias voltage relationship.

In order to determine the barrier height of the Au contact, C-V measurements were conducted on this diode at 1MHz. A typical $1/C^2$ vs. voltage curve is shown in Fig. 6. A very linear relationship was observed in this plot. The barrier height is expressed as (23)

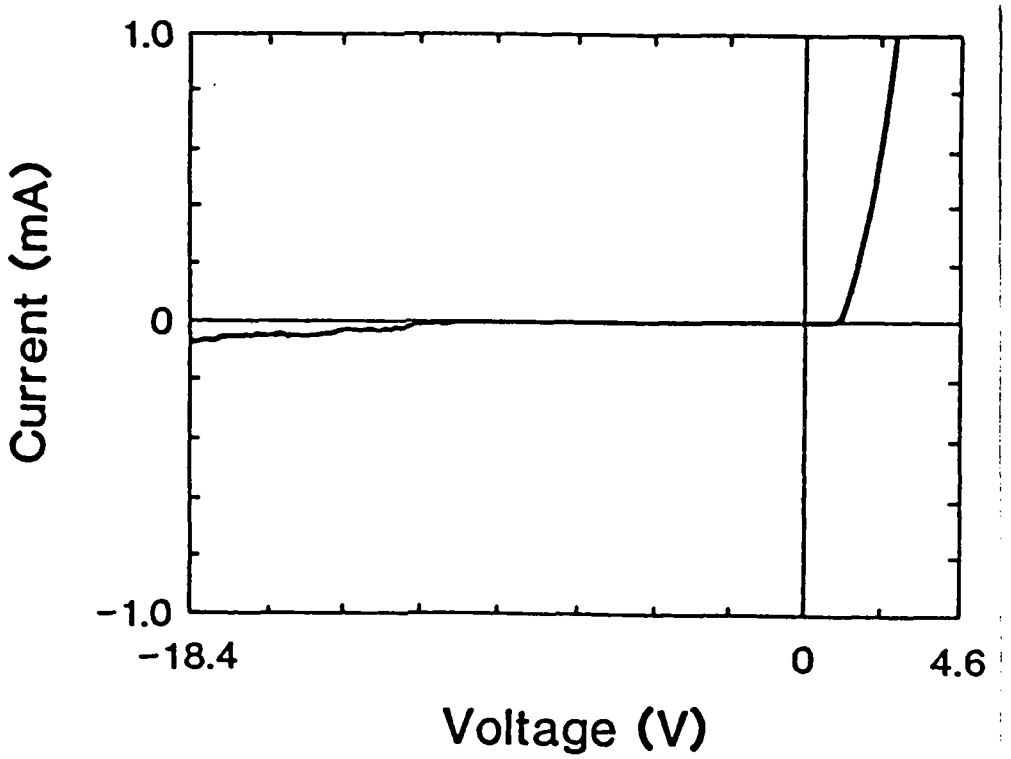

Fig. 5. I-V characteristics of Au-β-SiC Schottky diode. Sputtered $TaSi_2$ was used to make the ohmic contact.

$$\varphi_B = V_i + \psi + kT/q - \Delta\varphi \ ,$$

where V_i is the intercept of the extrapolated $1/C^2$ vs. V curve with the voltage axis, ψ is the depth of the Fermi level below the bottom of the conduction band, and $\Delta\varphi$ is the image force lowering of the barrier height at the interface. From Figure 6, it can be seen that V_i is approximately 1.1V. The value of ψ was determined to be 170 meV knowing the sample donor concentration ($n = 1 \times 10^{16}$ cm^{-3}), kT/q is 26meV at room temperature, and $\Delta\varphi$ is $\simeq$ 89mV (16). Therefore, the sum of all the terms in the right hand side of the above equation is 1.20V. Thus, the barrier height calculated from the capacitance measurements is 1.20V. The measured value of the barrier height for the Au-β-SiC junction above closely agrees with the values of 1.11-1.15V reported by Yoshida et. al. (18).

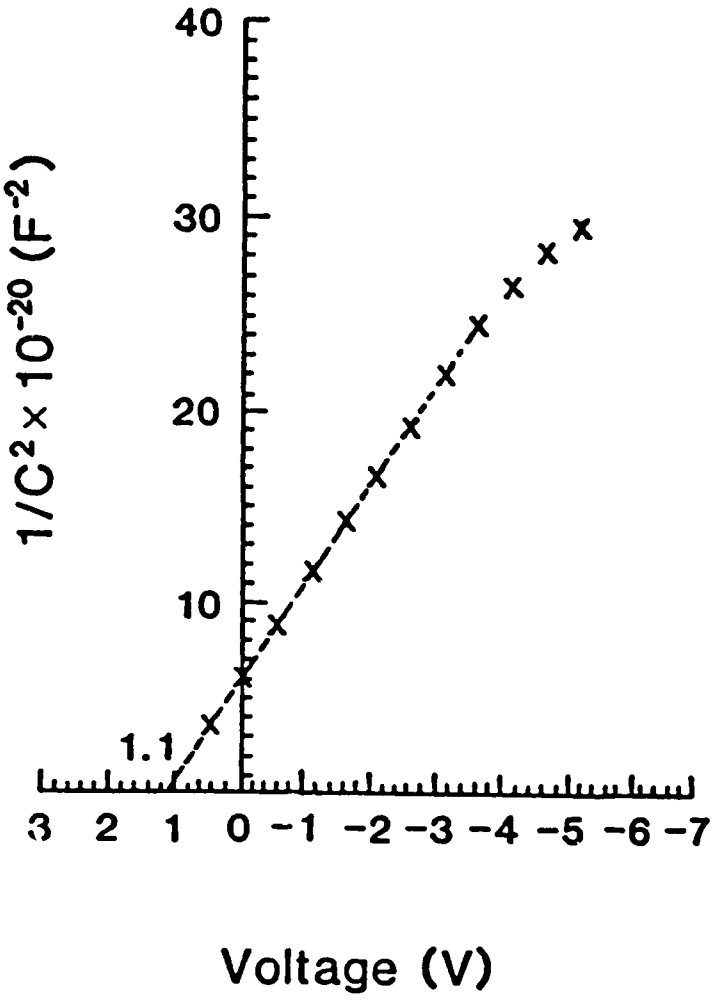

Fig. 6. Capacitance-voltage characteristics of Au-β-SiC Schottky diodes.

CONCLUSIONS

The contact properties of the commonly used as well as newly developed ohmic contacts have been studied. For n-type β–SiC, the contact properties of annealed Ni, Cr, Au-Ta and as-deposited Al were inferior to $TaSi_2$ annealed for 300 s at 1123K. The room temperature contact resistivity of this last material after annealing was 2.0×10^{-2} Ω-cm^2. For p-type β-SiC, good ohmic properties were obtained using elemental Al annealed at

1150K for 180 s. This resulted in a contact resistivity of 3.1×10^{-2} Ω - cm^2. It was shown that both $TaSi_2$ and Al were stable ohmic contacts to operating temperatures as high as 673K. At this temperature the contact resistivity decreased by a factor of two and ten, respectively.

Schottky barrier diodes using Au and $TaSi_2$ for rectifying and ohmic contacts, respectively, on n-type β-SiC were obtained. The barrier height of the Au contact was 1.20eV and the diode ideality factor was 2.1.

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IX. High Temperature Depletion Mode Metal-Oxide-Semiconductor Field-Effect Transistors in Beta-SiC Thin Films

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Abstract

Depletion mode n-channel metal-oxide-semiconductor field-effect transistors were fabricated on n-type β-SiC (111) thin films epitaxially grown by chemical vapor deposition on the Si (0001) face of 6H α-SiC single crystals. The gate oxide was thermally grown on the SiC; the source and drain were doped n^+ by N^+ ion implantation at 823K. Stable saturation and low subthreshold current was achieved at drain voltages, V_{DS}, exceeding 25 V. Transconductances as high as 11.9 mS/mm were achieved. Stable transistor action was observed at temperatures as high as 923K, the highest temperature reported to date for a transistor in any material.

The extreme thermal and chemical stability coupled with a bandgap of 2.2 eV (room temperature) are the primary reasons β-SiC continues to be investigated as a candidate semiconductor material for the fabrication of devices that can operate at temperatures exceeding 473K. Moreover, β-SiC also possesses a high electric breakdown field (4×10^6 V/cm) and a high saturated electron drift velocity (2.5×10^7 cm/sec) which allow concurrent high temperature, high power and/or high frequency operation of devices produced in this material[1].

Historically, device research on β-SiC has been very limited because of difficulty in obtaining high quality films. This research increased markedly following the development of a two-step method for growing β-SiC (100) on Si (100) substrates to relieve the respective 20% and 8% mismatches in lattice parameters and coefficients of thermal expansion. Specifically, this method consists of an initial conversion of the Si (100) surface to β-SiC via the reaction with C_2H_4 carried in H_2 followed by the introduction of SiH_4 and the consequent formation of β-SiC thin films[2,3]. High quality p-n junction diodes have been fabricated via sequential doping during growth[4] and by high temperature ion implantation[5]. Schottky diodes[6], as well as Schottky barrier field-effect transistors (MESFET's)[7,8], have been produced in these films. The MESFET's reported by Kong *et al.*[8] operated at temperatures to 623K, at which point leakage currents due to the generation current in the depletion region became significant.

Capacitance-voltage (C-V) measurements of metal-oxide-semiconductor (MOS) capacitors on β-SiC films grown on Si (100) have been reported using double column mercury probe[9] and conventional MOS structures[10]. An experimental depletion mode metal-oxide-semiconductor field-effect transistor (MOSFET) was fabricated in SiC by Kondo *et al.*[11], but it did not show any saturation characteristics nor did it sufficiently cut off. Inversion mode MOSFET's on β-SiC films on Si (100) have also been fabricated[12,13]. These devices exhibited saturation and cutoff to a drain-source voltage of about 4 V, where the leakage current began to dominate.

It is possible that the many stacking faults and the antiphase domain boundaries present in β-SiC (100) thin films grown on Si (100)[14] contribute to the leakage current by being paths of high conductivity. Recently, the concentrations of these defects have been greatly reduced by growing the β-SiC in the (111) orientation on 6H α-SiC (0001) substrates[15]. Moreover, the highest quality FET's ever reported in SiC have been fabricated in these latter films. The high temperature characteristics of these MOSFET's are described below.

The concentric ring device structure used in this research (identical to that shown in Fig. 2 of reference 8) contained a 100 μm diameter circular dot which functioned as the drain. This drain was entirely surrounded by a concentric gate ring having a 20 μm wide

connecting strip extending to a 100 μm x 100 μm contact pad. The source contact was an outer concentric semicircle that surrounded the gate ring except for the gate's connection strip. This source ring also had a connecting strip to a 100 μm diameter contact pad. The two different gate lengths used in this report were 7.2 μm and 2.4 μm.

The MOSFET's were fabricated in 1.2 μm thick n-type layers (n=1-3x10^{15} cm^{-3}) on ≈0.5 μm thick p-type β-SiC thin films grown by chemical vapor deposition at 1773K on the Si (0001) face of 6H α-SiC crystals. The thicknesses of these layers were determined by secondary ion mass spectrometry and spreading resistance measurements. The carrier concentrations of the n and p type layers were determined by MOS and differential C-V techniques, respectively. The source of p-type doping (p=1-6x10^{16} cm^{-3}) in the 0.5 μm p-type layer was Al which diffused from the heavily Al doped 6H α-SiC substrate during the three hour epilayer growth at 1773K. These acceptor species also highly compensated the n-type layers, thus producing the unusually low carrier concentration.

These films were polished using 0.1 μm diamond paste, heated in pure flowing O_2 at 1473K for 90 mins. to remove the polishing damage, and etched in HF to remove the resulting 43 nm oxide film. The gate oxide was subsequently grown at 1473K, again for 90 minutes, to yield 43 nm of SiO_2. A three-step cleaning process of hot H_2SO_4 (5 mins.), 1:1 mixture of hot NH_4OH and H_2O_2 (5 mins.),and

HF (1 min.), followed by a deionized water rinse, was used before each of these oxidation processes. A 500 nm thick film of polycrystalline silicon was deposited on the oxide via low pressure CVD at 893K, degenerately doped by P diffusion at 1173K for 5 min. and patterned photolithographically to form the gate contacts. The n^+ source and drain areas were then subsequently formed by dual (70 keV, 5.0×10^{14} cm^{-2}, and 40 keV, 3.35×10^{14} cm^{-2}), high temperature (773K), N^+ ion implantations through the oxide, with the 500 nm of polycrystalline silicon acting as an implant mask to give a self-aligned n^+-n-n^+ gate structure, as shown Fig. 1. Windows for the source and drain contacts were opened in the oxide via buffered oxide etch. Tantalum silicide was subsequently sputter deposited and pattered by the "lift-off" technique. The resulting contacts were then annealed at 1173K for 5 min. in vacuum. After making initial electrical measurements, the samples were then annealed in forming gas (10% H_2 in N_2) at 723K for 60 min. as a potential route to reduce oxide charge.

The drain current-voltage characteristics of a MOSFET in β-SiC (111) at 296K are shown in Fig. 2(a). This particular device had a gate length and width of 7.2 μm and 390 μm, respectively. The source contact to drain contact distance was 24 μm. The device showed very stable drain current saturation out to a drain-source voltage of 25 V. (This trend actually continued to $V_{DS} \approx 30$ V, at which point the oxides underwent breakdown.) This is the first time stable saturation has been reported for $V_{DS}>5$ V for any β-SiC FET. The threshold voltage was determined to be at a gate voltage, V_G, of

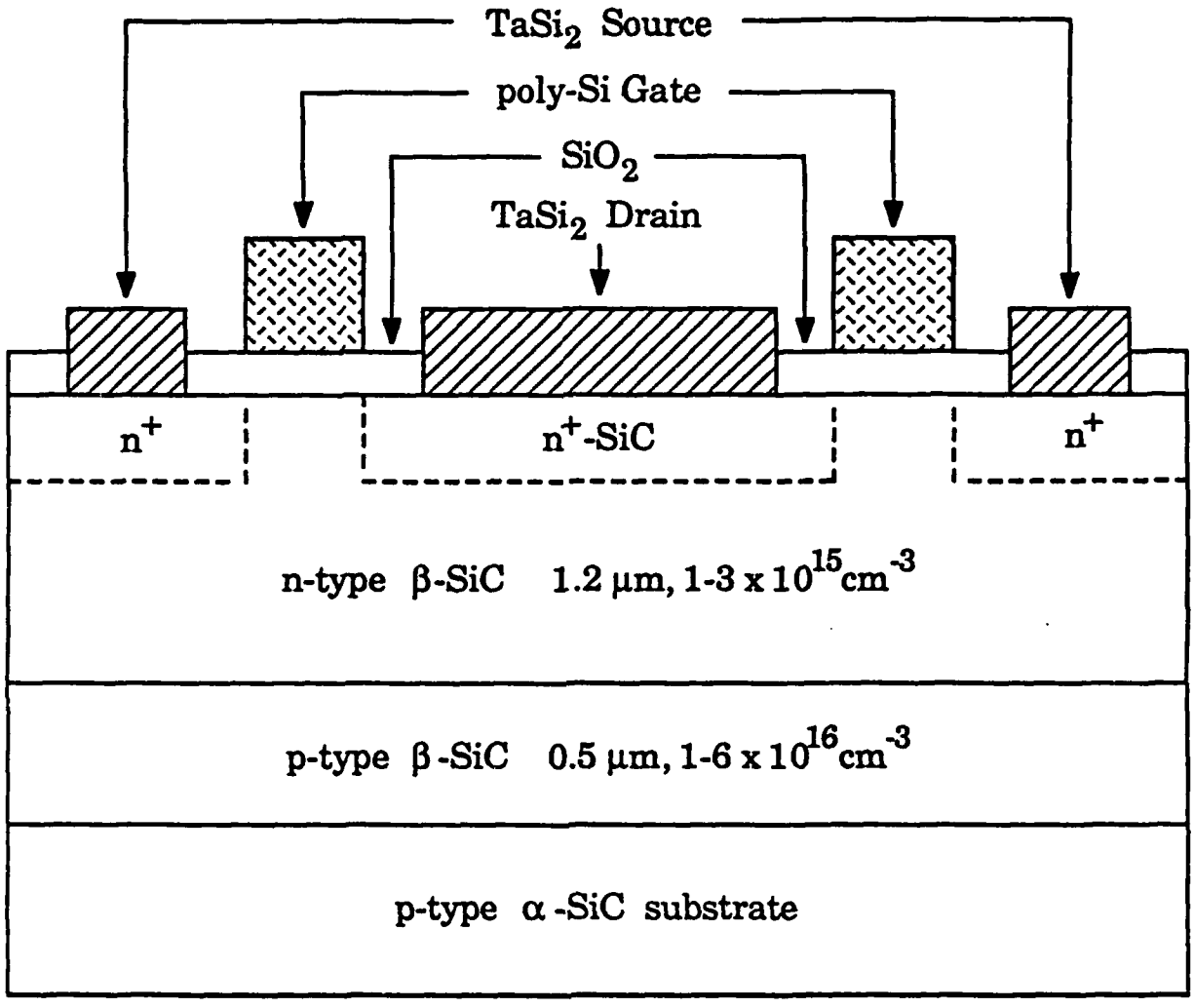

Figure 1. Cross-sectional view of the depletion mode MOSFET structure.

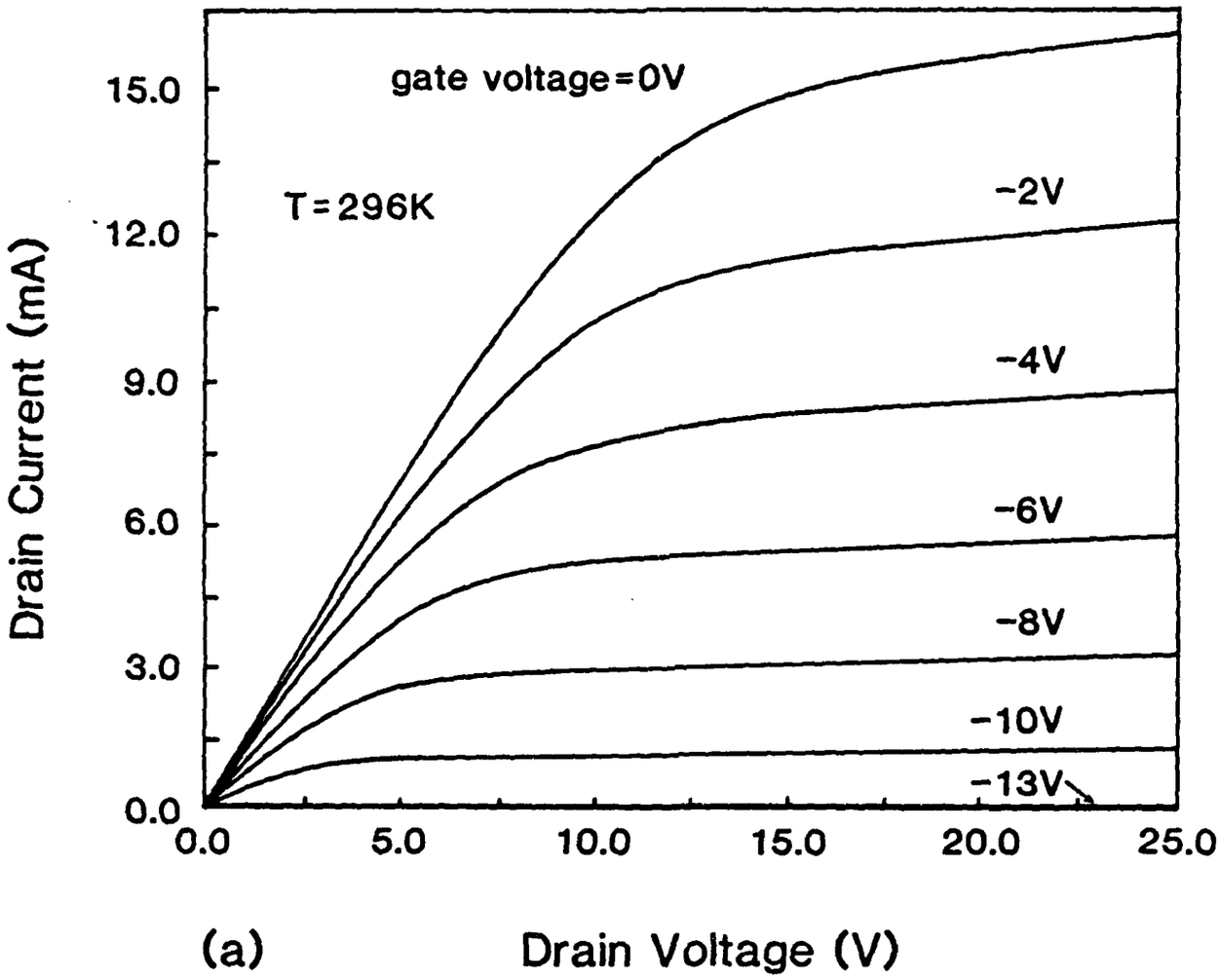

Figure 2a. Drain characteristics of depletion mode n-channel MOSFET in β-SiC (111) thin film at 296K. The gate length and width of this device was 7.2 m and 390 m, respectively.

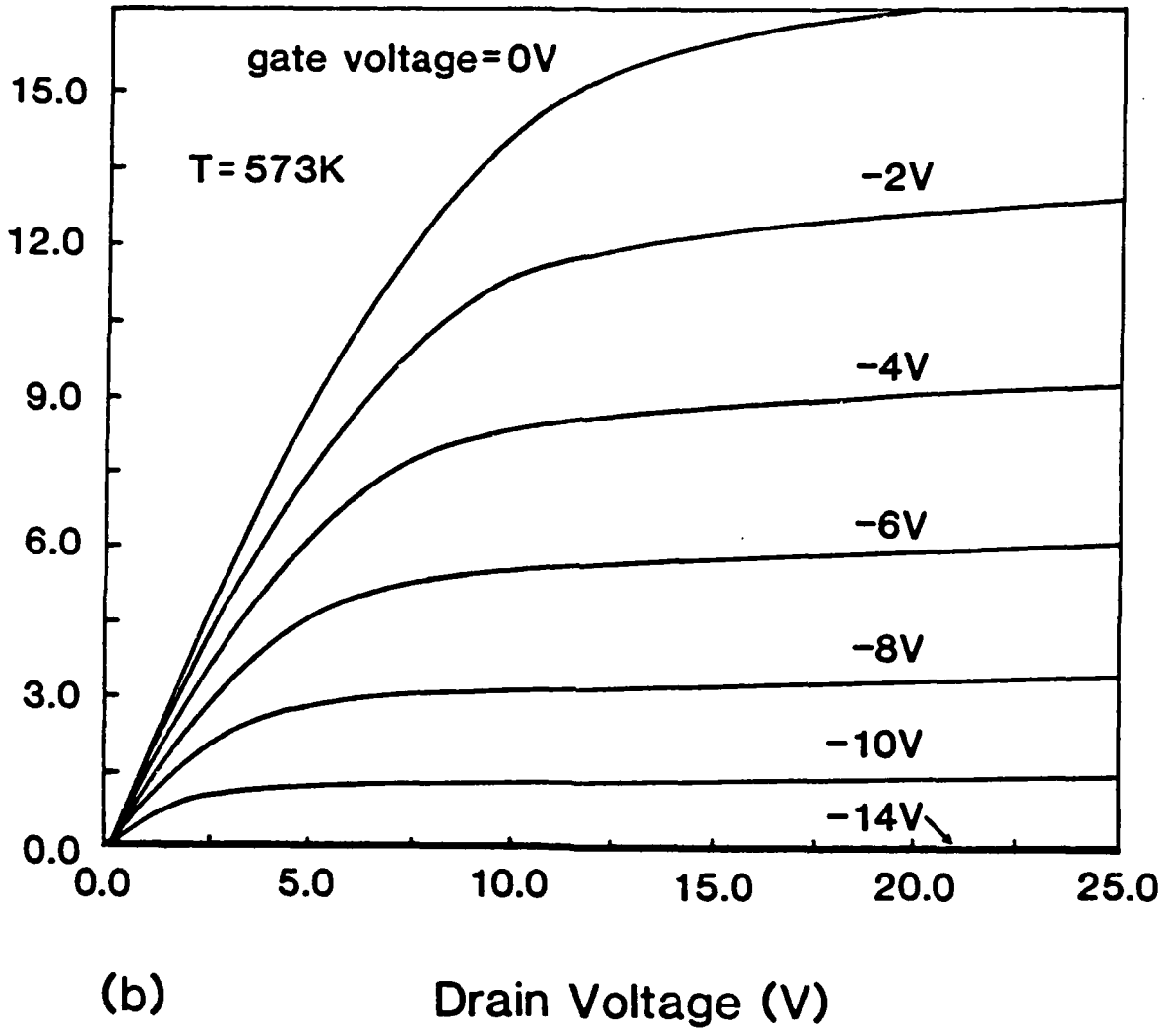

Figure 2b. Drain characteristics of depletion mode n-channel MOSFET in β-SiC (111) thin film at 923K. The gate length and width of this device was 7.2 m and 390 m, respectively.

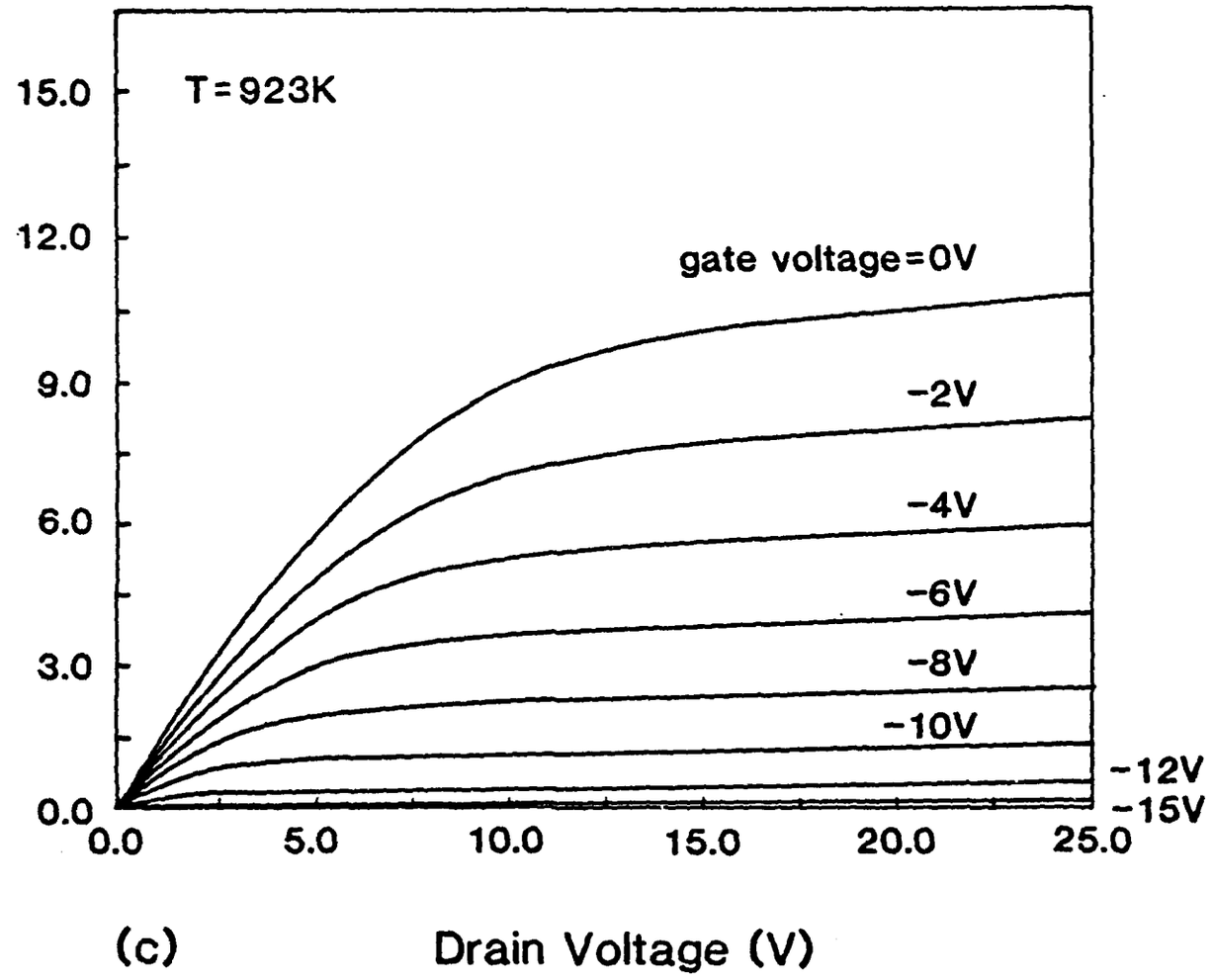

Figure 2c. Drain characteristics of depletion mode n-channel MOSFET in β-SiC (111) thin film at 923K. The gate length and width of this device was 7.2 m and 390 m, respectively.

-12.9 V from a plot of $\sqrt{I_{DS(sat)}}$ versus V_G. The leakage current at V_{DS}=25 V in the "off" state (V_G=-15 V) in this device was 3.75 μA. The negative threshold voltage was due, in part, to the voltage required to deplete the n-channel, but it was made more negative by the presence of either fixed oxide charge or mobile ion charge in the range of 5-6x10^{12} cm^{-2}, as obtained from MOS C-V curves of the gate oxide. The aforementioned 723K anneal in forming gas did not change the threshold voltage. The maximum transconductance of this device at room temperature with V_{DS} fixed at 20 V was 5.32 mS/mm at V_G=2.5 V.

When this device was heated to 573K and allowed to stabilize for 15 mins., the transconductance actually increased to a maximum of 6.00 mS/mm at V_G=5.5 V and V_{DS}=20 V. This trend can also be observed by the increased current at V_G=0 V in the 573K drain characteristics shown in Fig. 2(b). The reason for this increase is currently under investigation. Despite the increase in temperature, the drain current saturation was still very stable to V_{DS}=25 V. The leakage current at V_{DS}=25 V and V_G=-15 V increased to 22 μA, and the threshold voltage shifted negatively to V_G=-13.3 V.

The drain characteristics of this device were also determined at 673K and at every 50K interval to a maximum of 923K. Results for this last temperature are shown in Fig. 2(c). The transconductance remained unchanged at 673K; however, it decreased with further increases in temperature. The maximum transconductance measured

was 11.9 mS/mm in a 2.4 μm gate length device at 673K. The lower transconductance of the device at 923K is demonstrated in Fig.2(c) by the lower current at V_G=0 V, as compared with the previous curves. Although the transconductance at this temperature became very erratic above V_G=1 V, it reached a maximum of about 4.8 mS/mm at V_G=8 V and V_{DS}=20 V. The decrease in transconductance above 673K is due to increasing lattice scattering with temperature. The threshold voltage again shifted negatively, to V_G=-14.8 V at 923K. The leakage current increased to 128 μA at V_G=-15 V and V_{DS}=25 V. When the temperature was raised to 973K, this device showed similar current saturation , but the gate oxide experienced breakdown. Thus, current was being injected at the gate and the device could not be cut off.

In summary, depletion mode MOSFET's have been fabricated on β-SiC (111). For the first time, high temperature operation of these transistors was observed up to 923K. Stable saturation and channel cutoff was achieved throughout this temperature range at drain-source voltages exceeding 25 V. Transconductance increased with temperature to 573K, and decreased with temperature after 673K. The maximum transconductance observed was 11.9 mS/mm on a 2.4 μm channel device at 673K, the highest ever reported for any kind of SiC FET.

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x. Temperature dependence of the current-voltage characteristics of metal-semiconductor field-effect transistors in *n*-type β-SiC grown via chemical vapor deposition

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Metal-semiconductor field-effect transistors (MESFET's) have been fabricated in an unintentionally doped, *n*-type β-SiC thin film grown by chemical vapor deposition (CVD). This *n*-type layer was deposited on a monocrystalline *p*-type β-SiC (100) CVD layer previously grown on a *p*-type Si (100) substrate. The buried *p* layer allowed the devices to be fabricated several microns away from the SiC/Si interface region which contained numerous defects formed as a result of the poor lattice match and different coefficients of thermal expansion between SiC and Si. Thermally evaporated Au was utilized for the gate contact. Sputtered $TaSi_2$ was employed for the source and drain contacts. The gate lengths and channel depths of these MESFET's were 3.5 and 0.60 μm, respectively. Saturation of the drain currents was achieved at room temperature. Furthermore, the current-voltage characteristics, measured from 298 to 623 K for the first time, indicated that these MESFET's performed reasonably well throughout this temperature range. The maximum transconductance obtained was 1.6 mS/mm; the value of this parameter decreased with temperature.

Beta-SiC is a candidate material for high-temperature, high-speed, and high-power electronic devices because of its large band-gap energy (2.2 eV),[1] high saturated electron drift velocity (2×10^7 cm/S),[2] and high thermal conductivity (3.9 W/cm deg).[3] Therefore, metal-semiconductor field-effect transistor (MESFET) devices fabricated in this material have the potential for high-speed operation at elevated temperatures. These properties also indicate that high device packing densities are potentially achievable in β-SiC films.

The fabrication of field-effect transistors using SiC has been previously attempted by several investigators.[4-6] Muench and his co-workers[4] reported MESFET fabrication on bulk crystals of α-SiC in 1977. Although saturation of drain currents was achieved and the maximum transconductance reported was 1.75 mS/mm, it is now widely accepted that β-SiC is of greater interest for electronic devices due to its higher electron Hall mobility. The value of this parameter for β-SiC has been postulated from theoretical calculations to be greater than that of α-SiC over the temperature range of 300–1000 K.[7] Device research involving β-SiC[5,6] has been made possible by recent advances in the chemical vapor deposition (CVD) of reproducible, monocrystalline β-SiC thin films on Si (100) substrates.[8-11] Unfortunately, in both of these device studies, saturation of drain currents was not achieved. A possible cause of this was believed to be the leakage current through the β-SiC *p-n* junction between the active *n* layer and the buried *p* layer.[5,6] Other possible causes include the bypass leakage current from the drain to the source, the dense defects near the Si/β-SiC interface,[12] and the leakage current at the surface of the β-SiC film. It should be noted that none of these studies reported MESFET characteristics at elevated temperatures.

In this research, MESFET's were fabricated in an *n*-type β-SiC thin film epitaxially deposited on a 7-μm-thick buried *p*-type β-SiC layer previously grown on a Si (100) substrate via CVD. A schematic cross section of such a device is shown in Fig. 1. All layers were grown at 1633 K and 1 atm using a cold wall, vertical barrel-type, rf-heated CVD system. H_2 was used as the carrier gas and pure SiH_4 and C_2H_4 gases were used as Si and C sources, respectively. A detailed description of the growth procedures is given in Ref. 11. Trimethylaluminum (TMA) was used as the Al dopant source to obtain the *p*-type β-SiC buried layer. H_2 was bubbled through the TMA at 290 K to introduce it into the primary gas stream. This layer was used to (1) confine the current to a thin *n*-type active region and (2) move this active layer away from the dense defect region which extended approximately 3 μm from the interface into the grown film.[12,13]

Following the growth of the *p*-type layer each sample was removed from the reactor, polished with 0.1 μm diamond paste to remove the surface roughness and oxidized at 1473 K in flowing dry oxygen for 90 min to remove polishing-induced subsurface damage. The sample was then etched in HF to remove the oxide, reinserted in the chamber, and heated to 1633 K in flowing H_2 for 5 min to thermally etch the surface. The reactant gases of SiH_4 and C_2H_4 were

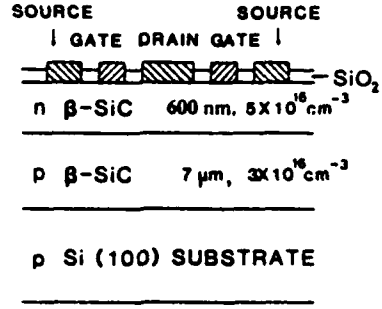

FIG. 1. Cross-sectional view of the MESFET structure.

[a] On assignment to NCSU from Kobe Development Corporation, Research Triangle Park, NC 27709.

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subsequently introduced into the growth chamber and allowed to flow for 17 min. This resulted in approximately 600 nm of an n-type layer which was employed as the active channel of the MESFET's. The carrier concentration of the n-type layers averaged approximately 5×10^{16} cm^{-3} and the hole concentration in the p-type layers was in the range of 3×10^{16}–3×10^{17} cm^{-3}. The sample examined for this letter has a hole concentration of 3×10^{16} cm^{-3} as determined by capacitance-voltage measurements with a Miller profiler. Finally, the sample was oxidized in flowing dry oxygen at 1373 K for 120 min to grow a 46-nm SiO_2 layer[14] to passivate the as-grown surface.

A three-level mask set employing a concentric ring geometry was used for fabrication of the MESFET's (Fig. 2). The gate pattern completely encloses the center (drain) contact which has a diameter of 100 μm. The gate contact pad is 100 μm on a side, and the outer (source) ring contact pad is 100 μm in diameter. The gate length and the source-to-drain distance are 3.5 and 10.5 μm, respectively. It was found that the reverse bias leakage current from the gate Schottky contact to the outer contact was much larger than that from the gate Schottky contact to the center contact. Therefore, the center contact was used as the drain since in the common source mode employed for these measurements, the gate-drain voltage is greater than the gate-source voltage. The difference in leakage current is believed to be due to the larger effective Schottky contact area present when measuring from the gate to the outer contact. The quality of the gate-source diode can probably be improved if the gate contact pad is located on top of the oxide layer rather than on the β-SiC surface. This configuration would reduce the effective rectifying contact area; however, this requires another mask level.

Sputtered $TaSi_2$ was used as the source and drain ohmic contacts. After sputtering, the sample was annealed at 1173 K for 5 min in vacuum in order to minimize contact resistance. Thermally evaporated Au was used as the gate rectifying contact. The MESFET structures were fabricated with conventional photolithography techniques. Two dark-field masks were used in conjunction with positive photoresist in order to open the ohmic and Schottky contact holes in the oxide layer while one bright-field mask and positive photoresist were used to etch the excess Au evaporated onto the oxide layer. The lift-off technique was used to remove excess $TaSi_2$ deposited on the SiO_2.

Typical room-temperature drain current versus drain voltage (I_D-V_D) characteristics of the MESFET's, obtained using a Hewlett Packard 4145A semiconductor parameter analyzer, are shown in Fig. 3. The gate voltage (V_G) was varied from 0.6 to -1.5 V in -0.3 V steps. It can be seen that very good drain current saturation is achieved as the drain voltage increases. The maximum transconductance in the saturated region for this device was 0.64 mS/mm; however, a maximum transconductance of 1.6 mS/mm was measured on other devices in this sample. The threshold voltage was -1.6 V, although after subtracting the leakage current, it is reduced to -1.4 V. It was observed that for $V_G < -2$ V the drain current was almost independent of the gate voltage, and thus the device could not be fully turned off. For example, for the device in Fig. 3, the drain current was 2 μA at a drain voltage of 4 V and a gate voltage < -2.5 V. This indicates that there is some leakage current between the gate and drain. This leakage may be caused by the p-n junction underneath the thin n layer, by the leakage current between the gate and source and/or by the defects in the β-SiC film. As previously reported,[12,13] the defect density, including the antiphase domain boundaries in the bulk of the film, is very high. Research is under way to fabricate MESFET's in films grown on α-SiC, since it has been shown that these films do not appear to contain any antiphase domain boundaries and much fewer line and planar defects than films grown on Si (100) substrates.[15] This will allow the determination of the role of these defects with regard to leakage current in the film.

MESFET's were also examined at temperatures to 623 K, a limit imposed by the maximum temperature of the experimental arrangement rather than the devices. Figure 4 shows examples of these measurements on the same device used to determine the room-temperature data of Fig. 3. In these measurements the drain voltage was applied from 0 to 10 V in order to more clearly illustrate the dependence of the I_D-V_D characteristics on temperature. Inset in these figures are the I-V characteristics of the gate-drain diode at the various temperatures. It can be seen that as the temperature was increased, the MESFET drain current achieved less saturation and the gate-drain diode (see inset) at reverse bias yielded more leakage current. At room temperature, this diode leakage current was 5 μA at 8.5 V reverse bias, whereas at 623 K it increased to approximately 70 μA. This was probably caused by an increase in the generation current in the

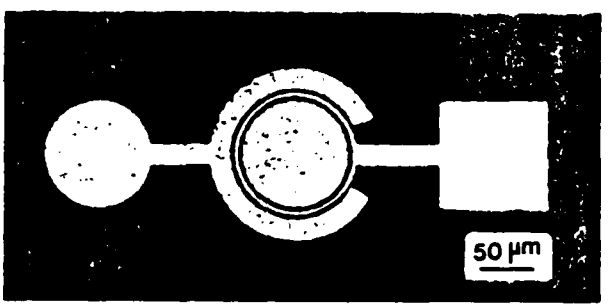

FIG. 2. Optical micrograph of a completed MESFET device on an n-type β-SiC layer. The gate length is 3.5 μm and the distance from drain to source is 10.5 μm.

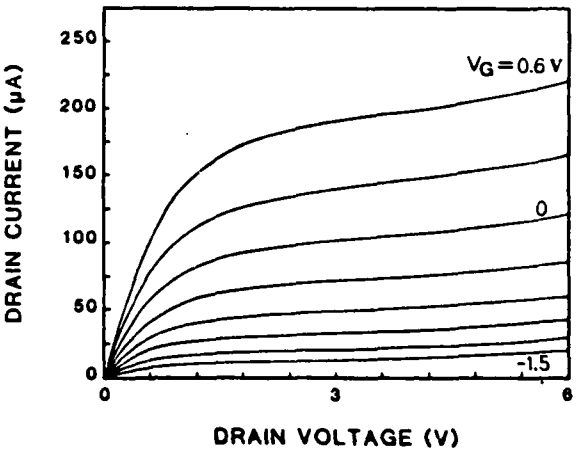

FIG. 3. Drain current-voltage characteristics at room temperature of a MESFET with a gate length of 3.5 μm.

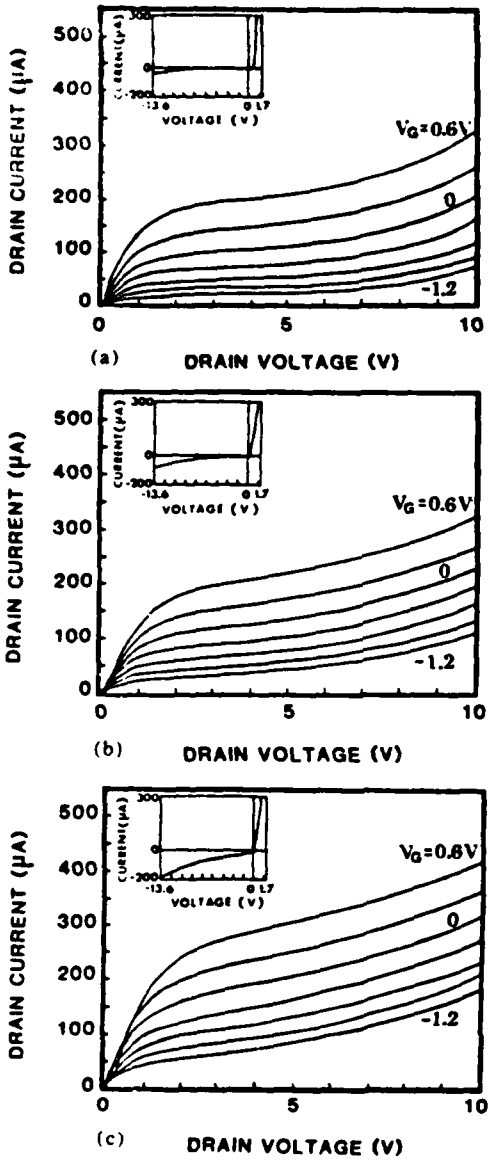

FIG. 4. Drain current-voltage characteristics of the MESFET used to obtain the data in Fig. 3: at (a) room temperature, (b) 473 K, and (c) 623 K. The current-voltage characteristics of the gate-drain Schottky diode are included as insets at each temperature.

depletion region as temperature was increased. These generated carriers also contribute to the drain-to-source leakage current. The maximum transconductance of this device decreased approximately 21%, as the temperature was increased to 623 K. This was expected because electron mobility decreases as temperature increases due to the enhanced lattice scattering.[16]

There are several factors, besides the gate length, which may influence the transconductance at a given temperature. They are (1) the source resistance consisting of the ohmic contact and bulk resistances of the source, (2) the Au/β-SiC interface roughness, (3) ionized impurities, and (4) defects. All of these factors affect the carrier mobility. In the present research, the interface roughness, as shown in Fig. 2, and the high defect densities of the antiphase domain boundaries, stacking faults and dislocations in the β-SiC, are the most probable factors which reduced the transconductance. The interface roughness probably affects the transconductance by contributing to the scattering of electrons in the channel; however, the growth of a thicker n-type layer and the polishing of the as-grown surface should reduce this problem. Furthermore, the use of β-SiC grown on α-SiC for the fabrication of MESFET's should eliminate any influence of the high defect density. Both of these aspects are currently under investigation.

In summary, MESFET's have been fabricated in a thin n-type β-SiC layer grown on a buried p-type β-SiC layer. These newly developed device structures made it possible for the drain current to reach saturation. Furthermore, the devices worked reasonably well up to 623 K; however, an increase in leakage current was observed as temperature was increased. The transconductance decreased approximately 21% as the temperature was increased from room temperature to 623 K. A maximum room-temperature transconductance of 1.6 mS/mm was measured. It is believed that utilizing an α-SiC substrate and polishing the n-channel surface prior to MESFET fabrication will further improve the I_D-V_D characteristics.

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